高效 Qi v1.1 兼容无线电源接收器和电池充电器

查询样品: **bq51050B**, **bq51051B**

特性

- 单级无线电源接收器
  和锂离子/锂聚合物电池充电器
  - 在一个单个小型封装内将无线电源接收器、整流器和电池充电器组合在一起
  - **4.2V** 和 **4.35V** 输出电压选项
  - 支持高达 **1.5A** 的充电电流
  - **93%** 峰值交流至直流 **(AC-DC)** 充电效率
- 稳健耐用架构
  - **20V** 最大输入电压耐受，
    具有输入过压 **(OV)** 保护钳位
  - 热关断和过流保护
  - 温度监控和故障检测
- 与无线充电联盟 **(WPC) v1.1 "Qi"** 工业标准兼容
- 功率级输出跟踪整流器和电池电压以确保整个充电周期内的最大效率
- 可提供小型晶圆级芯片尺寸封装 **(WCSP)** 和四方扁平无引线 **(QFN)** 封装

应用范围

- 电池组
- 手机与智能电话
- 耳机
- 便携式媒体播放器
- 其它手持式器件

说明

bq5105x 是一款高效、无线电源接收器，此接收器具有针对便携式应用的锂离子/锂聚合物电池充电控制器。bq5105x 器件提供高效 AC/DC 电源转换，集成了符合 Qi v1.1 通信协议所需的数字控制器以及高效且安全锂离子和锂聚合物电池充电器所要求的全部控制算法。 与 bq500210 发送器侧控制器组合在一起，bq5105x 可实现一个针对直接电池充电器解决方案的完整无线电源传输系统。 通过采用近场电感电源传输，嵌入在便携式器件内的接收器线圈能够接收到发送器线圈所发出的电源。 然后，来自接收器线圈的 AC 信号被整流和调节以将电源直接应用于电池。 为了稳定电能传输过程，建立了接收器到发送器的全局反馈。 这个反馈由 Qi v1.1 通信协议建立。

bq5105x 器件在单个封装内集成了一个低阻抗同步整流器、低压降稳压器、数字控制、充电器控制器和精准电压和电流环路。 整个功率级（整流器与 LDO）均采用低阻性 N 通道金属氧化物半导体场效应晶体管 (N-MOSFET)（导通电阻 (Rdson) 典型值 100mΩ）技术以确保高效率与低功率耗散。

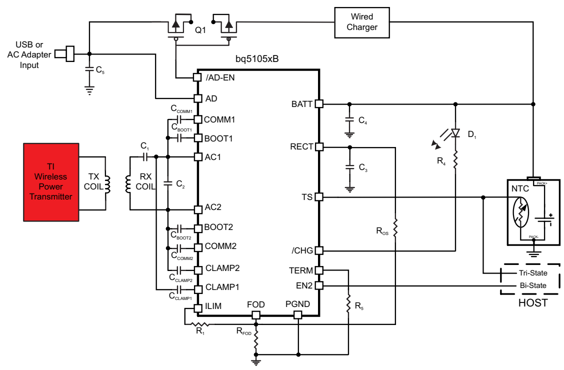


图 **1.** 典型系统方框图显示 **bq5105xB** 被用作一个无线电源锂离子/锂聚合物电池充电器

请注意：请访问ti.com/wirelesspower以获取产品详细信息和设计资源

English Data Sheet: SLUSB42

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NO.	IC MARKING	PACKAGE	ORDERING NUMBER (TAPE AND REEL)	QUANTITY
bq51050B	bq51050B	WCSP-28	bq51050BYFPR bq51050BYFPT	3000 250
	bq51050B	VQFN-20	bq51050BRHLR bq51050BRHLT	3000 250
bq51051B	bq51051B	WCSP-28	bq51051BYFPR bq51051BYFPT	3000 250
	bq51051B	VQFN-20	bq51051BRHLR bq51051BRHLT	3000 250

AVAILABLE OPTIONS

DEVICE	FUNCTION	$V_{RECT-OVP}$	$V_{RECT(REG)}$	$V_{BAT(REG)}$	NTC MONITORING
bq51050B	4.2V Li-Ion Wireless Battery Charger	15V	Track	4.2V	JEITA
bq51051B	4.35V Li-Ion Wireless Battery Charger	15V	Track	4.35V	JEITA

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUES		UNITS
		MIN	MAX	
Input voltage	AC1, AC2, RECT, COMM1, COMM2, BAT(OUT), $\overline{CHG}$, CLAMP1, CLAMP2	–0.3	20	V
	AD, AD-EN	–0.3	30	V
	BOOT1, BOOT2	–0.3	26	V
	EN2, TERM, FOD, TS-CTRL, ILIM	–0.3	7	V
Input current	AC1, AC2		2	A(RMS)
Output current	BAT(OUT)		1.5	A
Output sink current	$\overline{CHG}$		15	mA
	COMM1, COMM2		1.0	A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–65	150	°C
ESD Rating	Human body model (HBM)(100pF, 1.5kΩ)		2	kV
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the VSS terminal, unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		YFP 28-PINS	RHL 20-PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	58.9	37.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	35.5	
θ_{JB}	Junction-to-board thermal resistance	9.1	13.6	
ψ_{JT}	Junction-to-top characterization parameter	1.4	0.5	
ψ_{JB}	Junction-to-board characterization parameter	8.9	13.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	2.7	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range	RECT	4.0	10.0	V
I_{IN}	Input current	RECT		1.5	A
I_{BAT}	BAT(output) current	BAT		1.5	A
$I_{AD\text{-}EN}$	Sink current	AD-EN		1	mA
I_{COMM}	COMM sink current	COMM		500	mA
T_J	Junction temperature		0	125	°C

TYPICAL APPLICATION SCHEMATIC

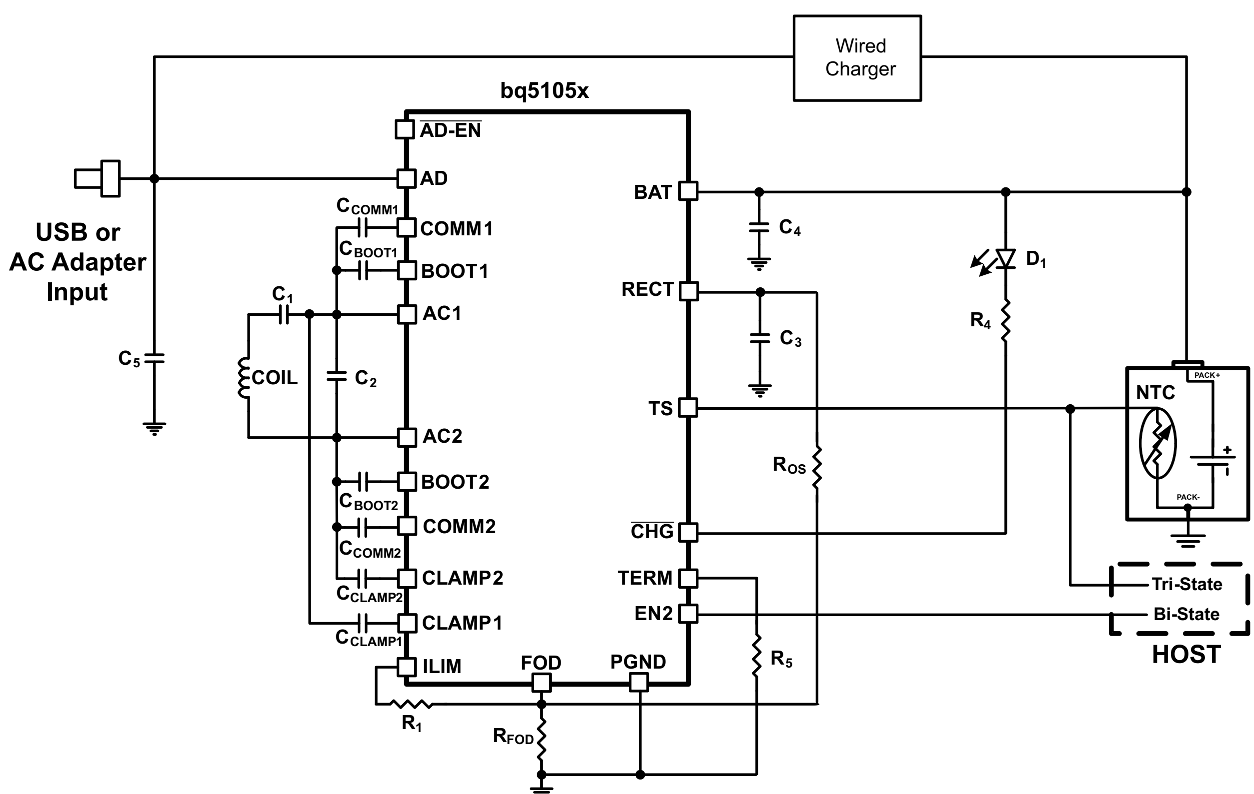


Figure 2. bq5105x Used as a Wireless Power Receiver and Li-Ion/Li-Pol Battery Charger

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Under-voltage lock-out	V_{RECT}: 0V → 3V	2.6	2.7	2.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{RECT}: 3V → 2V		250		mV
	Hysteresis on OVP	V_{RECT}: 16V → 5V		150		mV
V_{RECT}	Input over-voltage threshold	V_{RECT}: 5V → 16V	14.5	15	15.5	V
$V_{RECT-REG}$ (1)	V_{RECT} regulation voltage			5.11		V
I_{LOAD}	I_{LOAD} Hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling		5%		
V_{TRACK}	Tracking V_{RECT} regulation above V_{BAT}	V_{BAT} = 3.5 V, I_{BAT} ≥ 500mA		300		mV
$V_{RECT-REV}$	Rectifier reverse voltage protection at the BAT(output)	$V_{RECT-REV} = V_{BAT} – V_{RECT}$, V_{BAT} = 10V		8.3	9	V
$V_{RECT-DPM}$	Rectifier under voltage protection, restricts I_{BAT} at $V_{RECT-DPM}$		3	3.1	3.2	V
QUIESCENT CURRENT						
I_{RECT}	Active chip quiescent current consumption from RECT (in the prswireless power is present)	I_{BAT} = 0, 0°C ≤ T_J ≤ 85°C		8	10	mA
		I_{BAT} = 300mA, 0°C ≤ T_J ≤ 85°C		2	3	mA
I_Q	Quiescent current at the BAT when wireless power is disabled(Standby)	V_{BAT} = 4.2V, 0°C ≤ T_J ≤ 85°C		12	20	µA
ILIM SHORT PROTECTION						
$R_{ILIM-SHORT}$	Highest value of I_{LIM} resistor considered a fault (short). Monitored for I_{BAT} > 100 mA	R_{ILIM}: 200 Ω → 50 Ω. I_{BAT} latches off, cycle power to reset			120	Ω
$t_{DGL-Short}$	Deglitch time transition from I_{LIM} short to I_{BAT} disable			1		ms
I_{LIM_SC}	$I_{LIM-SHORT,OK}$ enables the I_{LIM} short comparator when I_{BAT} is greater than this value	I_{BAT}: 0 → 200 mA	110	145	165	mA
$I_{LIM-SHORT, OK HYSTERESIS}$	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{BAT}: 200 → 0 mA		30		mA
I_{BAT-CL}	Maximum output current limit	Maximum I_{BAT} that will be delivered for 1 ms when ILIM is shorted			2.4	A
BATTERY SHORT PROTECTION						
$V_{BAT(SC)}$	BAT pin short-circuit detection/pre-charge threshold	V_{BAT}: 3 V → 0.5 V, no deglitch	0.75	0.8	0.85	V
$V_{BAT(SC)-HYS}$	$V_{BAT(SC)}$ hysteresis	V_{BAT}: 0.5 V → 3 V		100		mV
$I_{BAT(SC)}$	Source current to BAT pin during short-circuit detection	V_{BAT} = 0V	12	18	22	mA
PRECHARGE						
V_{LOWV}	Pre-charge to fast charge transition threshold	V_{BAT}: 2 V → 4 V	2.9	3.0	3.1	V
K_{PRECHG}	Pre-charge current as a percentage of I_{BAT}	$V_{LOWV} > V_{BAT} > V_{BAT(SC)}$, I_{BAT}: 50 – 300 mA	18%	20%	23%	
$t_{pre-charge}$	Pre-charge timeout	$V_{BAT}<V_{LOWV}$		30		min
$t_{DGL1(LOWV)}$	De-glitch time, pre- to fast-charge			25		ms
$t_{DGL2(LOWV)}$	De-glitch time, fast- to pre-charge			25		ms
TIMERS						
$T_{fast-charge}$	Fast-charge timer	$V_{LOWV} < V_{BAT} < V_{BAT(REG)}$		36000		sec
$T_{pre-charge}$	Pre-charge timer	$V_{BAT-SHORT} < V_{BAT} < V_{LOWV}$		1800		sec
OUTPUT						
V_{OREG}	Regulated BAT(output) voltage	I_{BAT} = 1000 mA, bq51050B	4.16	4.2	4.22	V
		I_{BAT} = 1000 mA, bq51051B	4.30	4.35	4.37	V
V_{DO}	Drop-out voltage, RECT to BAT	I_{BAT} = 1A		110	190	mV
K_{ILIM}	Current programming factor	$R_{LIM} = K_{ILIM} / I_{ILIM}$	290	300	320	AΩ
I_{BAT}	Battery charge current limit programming range				1500	mA
$I_{COMM-CL}$	Current limit during communication		330	390	420	mA

(1) $V_{RECT(REG)}$ is over ridden when rectifier fold back mode is active ($V_{RECT(REG)-TRACKING}$).

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TERMINATION							
K_{TERM}	Programmable termination current as a percentage of I_{ILIM}	R_{TERM} = %I_{ILIM} x K_{TERM}		200	240	280	Ω/%
I_{TERM}	Constant current at the TERM pin to bias the termination reference			40	50	55	µA
V_{RECH}	Recharge threshold		bq51050B	$V_{BAT(REG)}$ –135mV	$V_{BAT(REG)}$ –110mV	$V_{BAT(REG)}$ –90mV	V
			bq51051B	$V_{BAT(REG)}$ –125mV	$V_{BAT(REG)}$ –95mV	$V_{BAT(REG)}$ –70mV	
TS / CTRL							
V_{TS}	Internal TS bias voltage	$I_{TS\text{-}Bias}$ < 100 µA (periodically driven see $t_{TS/CTRL\text{-}Meas}$)		2	2.2	2.4	V
V_{OC}	Rising threshold	VTS: 50% → 60%		57	58.7	60	%V_{TSB}
	Falling threshold	VTS: 60% → 50%		55	56.3	57	
	Hysteresis on 0C Comparator	VTS: 60% → 50%			2.4		
V_{10C}	Rising threshold	VTS: 40% → 50%		46	47.8	49	%V_{TSB}
$V_{10C\text{-}Hyst}$	Hysteresis on 10C Comparator	VTS: 50% → 40%			2		%V_{TSB}
V_{45C}	Falling threshold	VTS: 25% → 15%		18	19.6	21	%V_{TSB}
$V_{45C\text{-}Hyst}$	Hysteresis on 45C Comparator	VTS: 15% → 25%			3		%V_{TSB}
V_{60C}	Falling threshold	VTS: 20% → 5%		12	13.1	14	%V_{TSB}
$V_{60C\text{-}Hyst}$	Hysteresis on 60C Comparator	VTS: 5% → 20%			1		%V_{TSB}
I_{45C}	I_{LIM} reduction percentage at 45c	VTS: 25% → 15%, I_{LOAD} = I_{ILIM}		45	50	55	%
$V_{CTRL\text{-}HI}$	CTRL pin threshold for a high	$V_{TS/CTRL}$: 50 → 150 mV		80	100	130	mV
$V_{CTRL\text{-}LOW}$	CTRL pin threshold for a low	$V_{TS/CTR}$L: 150 → 50 mV		50	80	100	mV
$T_{TS/CTRL\text{-}Meas}$	Time period of TS/CTRL measurements--when VTSB is being driven	TS bias voltage is only driven when communication packets are sent			24		ms
$t_{TS\text{-}Deglitch}$	Deglitch time for all TS comparators				10		ms
NTC-Pullup	Pull-up resistor for the NTC network. Pulled up to the TS bias LDO.			18	20	22	kΩ
NTC-R_{NOM}	Nominal resistance requirement at 25c of the NTC resistor				10		kΩ
NTC-Beta	Beta requirement for accurate temperature sensing via the above specified thresholds				3380		Ω
THERMAL PROTECTION							
T_J	Thermal shutdown temperature				155		°C
	Thermal shutdown hysteresis				20		°C
OUTPUT LOGIC LEVELS ON /CHG							
V_{OL}	Open drain $\overline{CHG}$ pin	I_{SINK} = 5 mA				500	mV
$I_{OFF,CHG}$	$\overline{CHG}$ leakage current when disabled	V_{CHG} = 20 V, 0°C ≤ T_J ≤ 85°C				1	µA
COMM PIN							
$R_{DS\text{-}ON(COMM)}$	Comm1 and Comm2	V_{rect} = 2.6V			1		Ω
f_{COMM}	Signaling frequency on COMM pin				2.00		Kb/s
$I_{OFF,Comm}$	Comm pin leakage current	V_{COMM1} = 20 V, V_{COMM2} = 20 V				1	µA
CLAMP PIN							
$R_{DS\text{-}ON(CLAMP)}$	Clamp1 and Clamp2				0.75		Ω

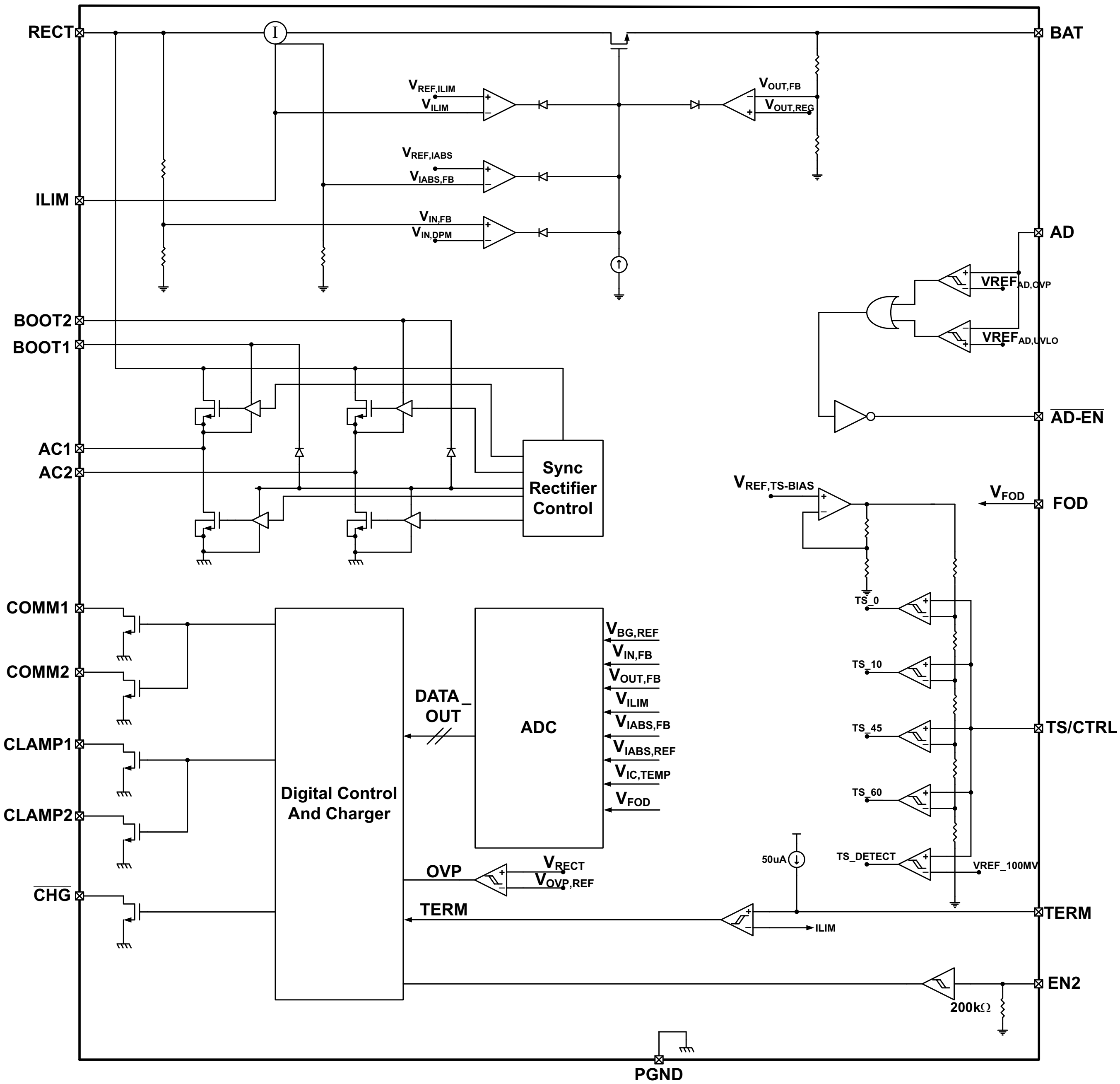
ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

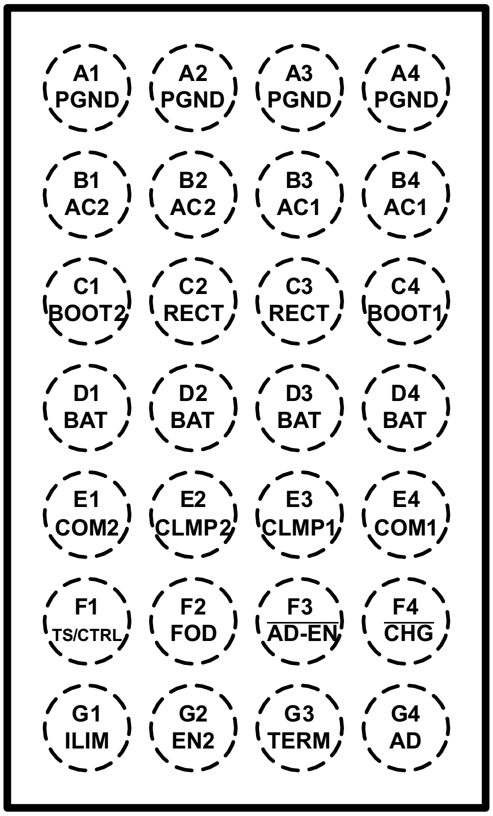
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS RECTIFIER						
I_{BAT}	I_{BAT} at which the synchronous rectifier enters half synchronous mode, SYNC_EN	I_{BAT} 200 → 0 mA	80	115	140	mA
	Hysteresis for $I_{BAT,RECT-EN}$ (full-synchronous mode enabled)	I_{BAT} 0 → 200 mA		25		mA
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250 mA, and T_J = 25°C		0.7		V
EN2						
V_{IL}	Input low threshold for EN2				0.4	V
V_{IH}	Input high threshold for EN2		1.3			V
$R_{PD, EN}$	EN2 pull down resistance			200		kΩ
ADC						
$P_{owerREC}$	Received power measurement	0W – 5W received power after calibration of Rx magnetics losses		0.25		W

DEVICE INFORMATION

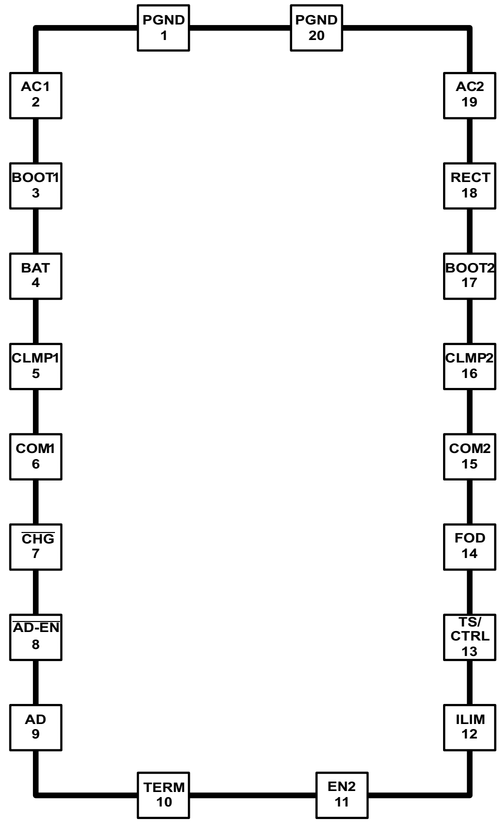
SIMPLIFIED BLOCK DIAGRAM



YFP Package
3.0mm x 1.9mm 28-Pin WCSP
(TOP VIEW)



RHL Package
4.35mm x 3.35mm 20-Pin QFN
(TOP VIEW)



PIN FUNCTIONS

NAME	WCSP	QFN	I/O	DESCRIPTION
AC1	B3, B4	2	I	Input power from receiver coil.
AC2	B1, B2	19	I	
BOOT1	C4	3	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
BOOT2	C1	17	O	
RECT	C2, C3	18	O	Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be 4.7μF to 22μF.
BAT	D1, D2, D3, D4	4	O	Output pin, delivers power to the battery while applying the internal charger profile.
COM1	E4	6	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COMM2 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COMM1 and COMM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation.
COM2	E1	15	O	Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COMM1 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COMM1 and COMM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation.
CLMP1	E3	5	O	Open drain FETs which are utilized for a non-power dissipative over-voltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the IC from damage. If used, Clamp1 is required to be connected to AC1, and Clamp2 is required to be connected to AC2 via 0.47μF capacitors.
CLMP2	E2	16	O	
PGND	A1, A2, A3, A4	1, 20	–	Power ground

PIN FUNCTIONS (continued)

NAME	WCSP	QFN	I/O	DESCRIPTION
ILIM	G1	12	I/O	Programming pin for the battery charge current. Connect external resistor to VSS. Size R_{ILIM} with the following equation: R_{ILIM} = 300 / I_{ILIM} where I_{ILIM} is the desired battery charge current.
AD	G4	9	I	Connect this pin to the wired adapter input. When a voltage is applied to this pin wireless charging is disabled and AD_EN is driven low. Connect to GND through a 1µF capacitor. If unused, capacitor is not required and should be grounded directly.
$\overline{\text{AD-EN}}$	F3	8	O	Push-pull driver for external PFET when wired charging is active.
TS/CTRL	F1	13	I	Must be connected to ground via a NTC resistor. If an NTC function is not desired, connect to GND with a 10 kΩ resistor. As a CTRL pin pull to ground to send end power transfer (EPT) fault to the transmitter or pull-up to an internal rail (i.e. 1.8 V) to send EPT termination to the transmitter.
TERM	G3	10	I	Input that allows the termination threshold to be programmable. K_{TERM} = 240 Ω/%. Set the termination threshold by applying the following equation R_{TERM} = %I_{ILIM} × K_{TERM} where %I_{ILIM} is the desired percentage of fast charge current when termination should occur.
EN2	G2	11	I	EN2=0 enables wired charging source if AD input volatge is above 3.6V, wireless charging is enabled if AD input volatge is < 3.6V, EN2=1 disables wired charging source; wireless power is always enabled if present.
FOD	F2	14	I	Input for the rectified power measurement. Connect to GND with a 188 Ω resistor.
$\overline{\text{CHG}}$	F4	7	O	Open-drain output – active when charging of the battery is active.

TYPICAL CHARACTERISTICS

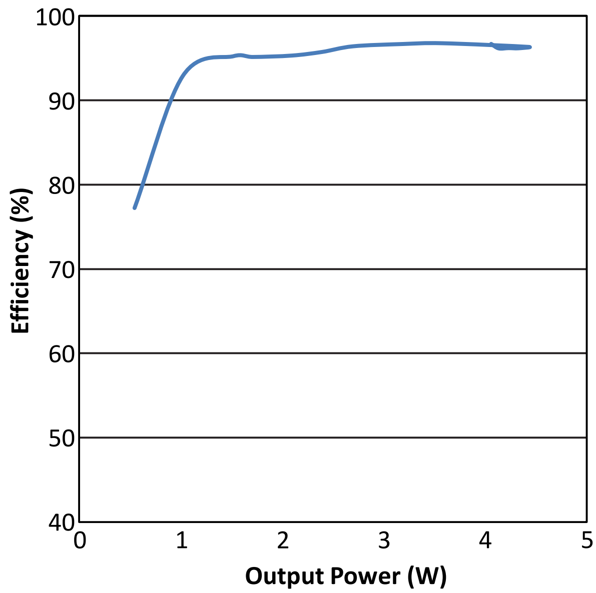


Figure 3. Rectifier Efficiency

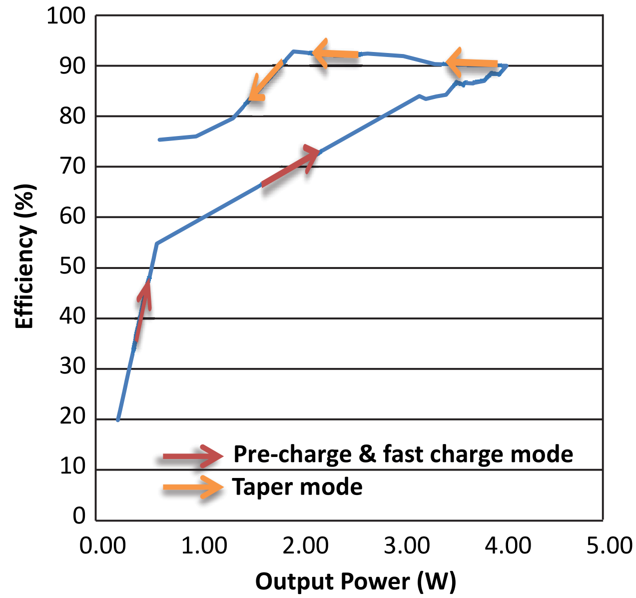


Figure 4. IC Efficiency (AC input to DC output)

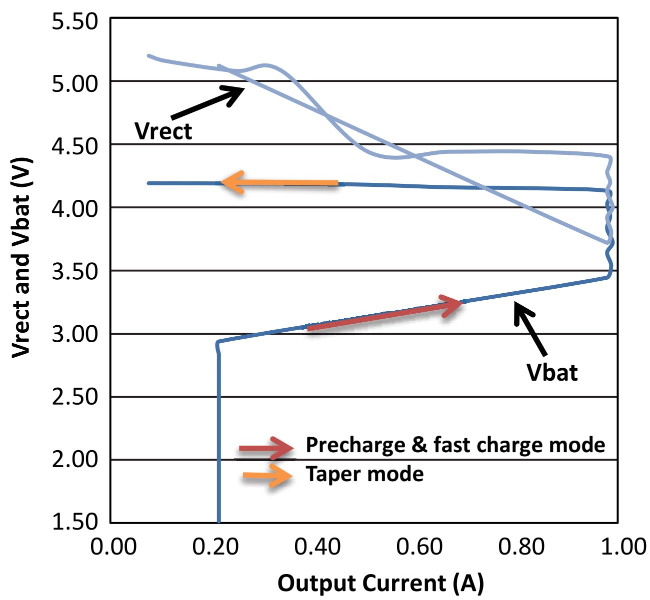


Figure 5. Vrect, Vbat Vs Output Current

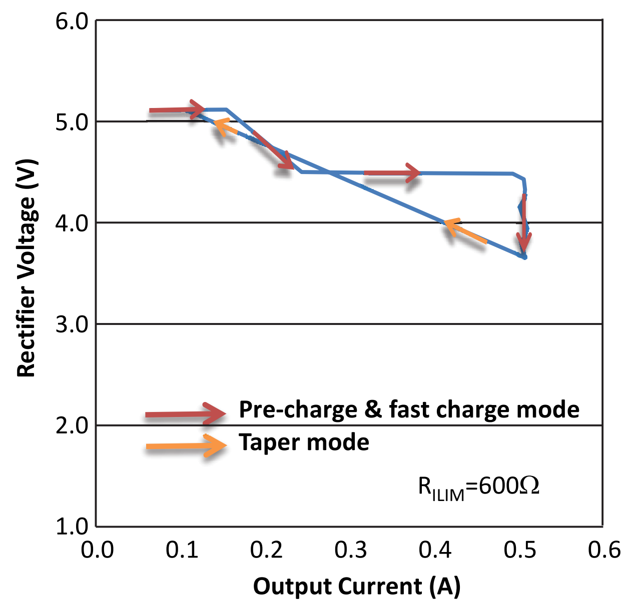


Figure 6. Vrect vs Output Current at R_{ILIM}=600Ω

TYPICAL CHARACTERISTICS (continued)

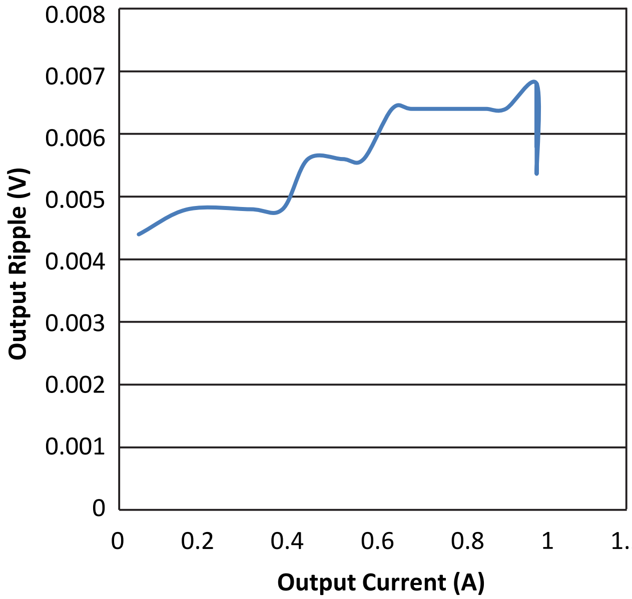


Figure 7. Output Ripple vs Output Current

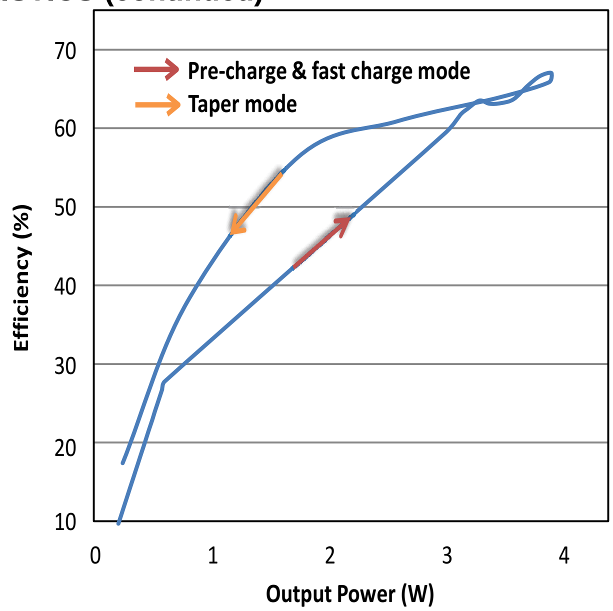


Figure 8. System Efficiency (DC input to DC output)

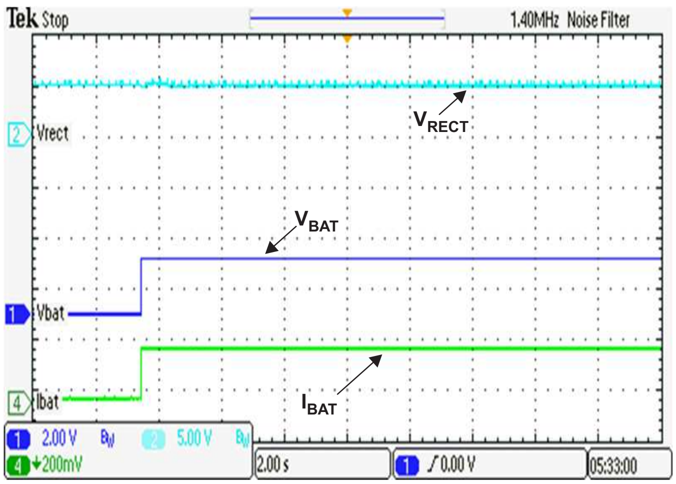


Figure 9. Battery Insertion in Pre-Charge Mode

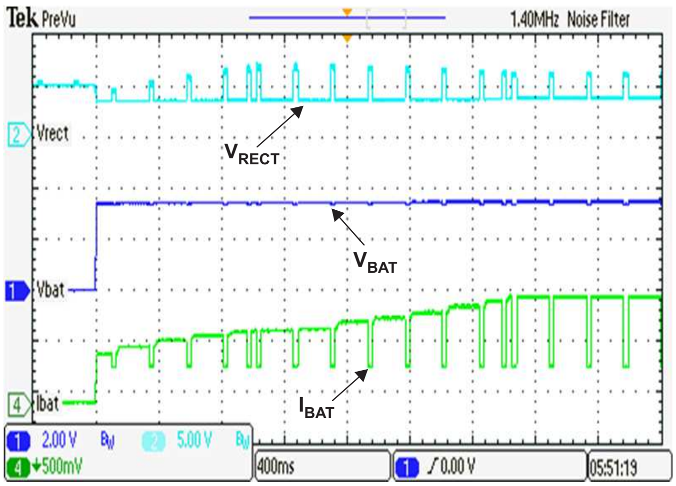


Figure 10. Battery Insertion in Fast-Charge Mode

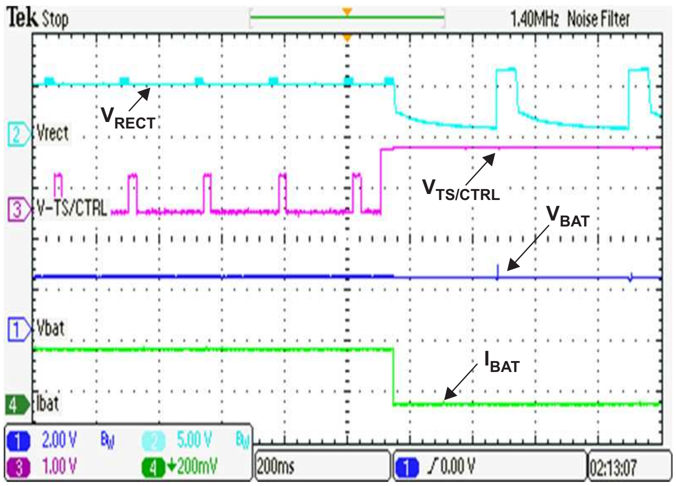


Figure 11. TS Fault

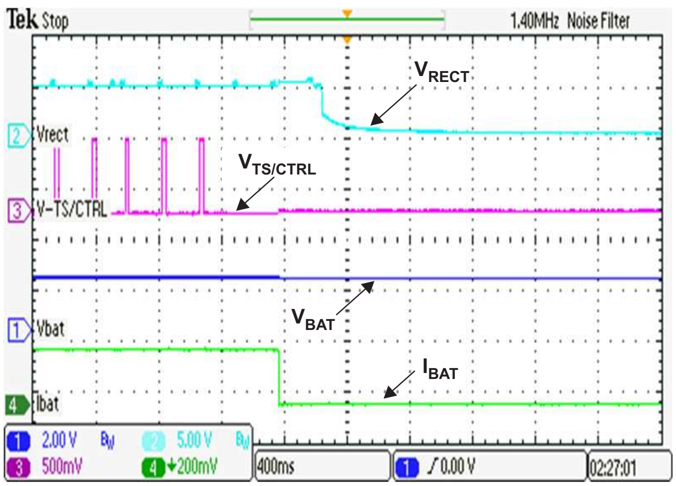


Figure 12. TS Ground Fault

TYPICAL CHARACTERISTICS (continued)

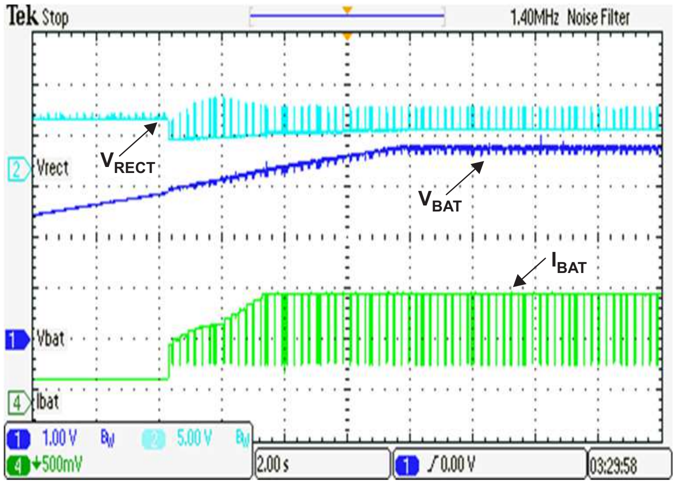


Figure 13. Pre-Charge to Fast Charge Transition

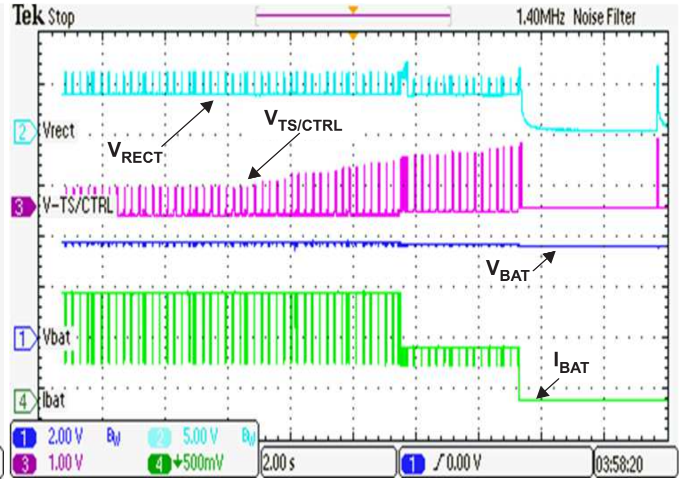


Figure 14. JEITA Functionality (Rising Temp)

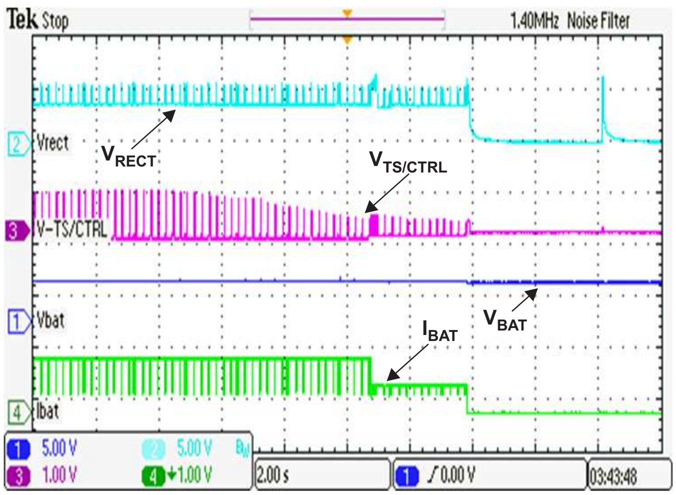


Figure 15. JEITA Functionality (Falling Temp)

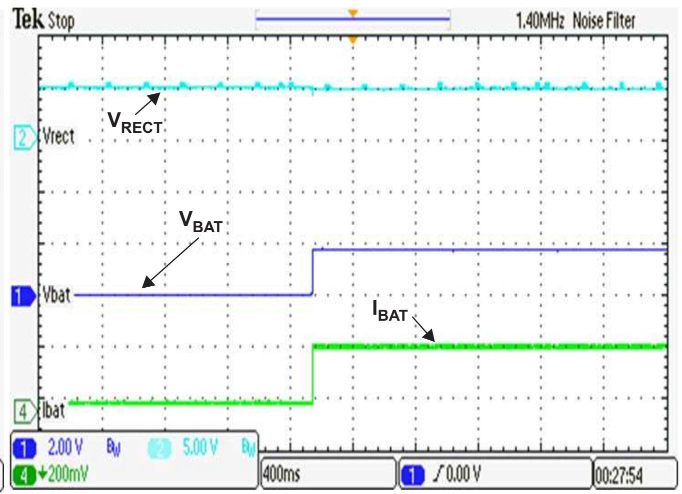


Figure 16. Battery Short to Pre-Charge Mode Transition

PRINCIPLE OF OPERATION

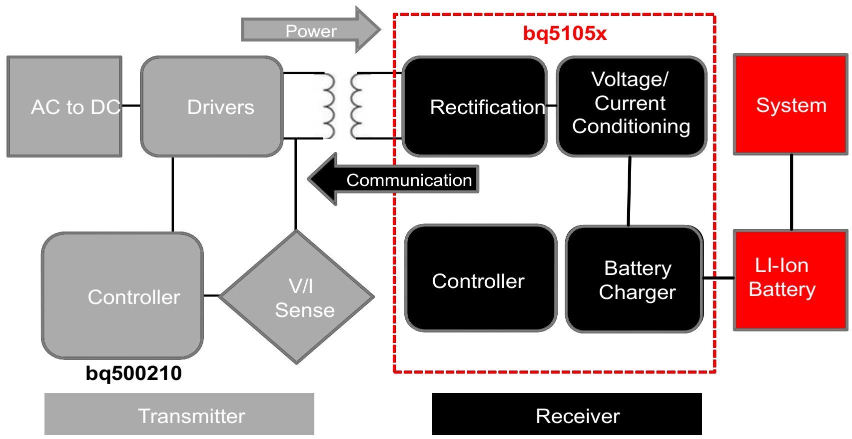


Figure 17. WPC Wireless Power Charging System Indicating the Functional Integration of the bq5105x

A Brief Description of the Wireless System

A wireless system consists of a charging pad (primary, transmitter) and the secondary-side equipment. There are coils in the charging pad and in the secondary equipment which magnetically coupled to each other when the equipment is placed on the charging pad. Power is transferred from the primary to the secondary by transformer action between the coils. Control over the amount of power transferred is achieved by changing the frequency of the primary drive.

The secondary can communicate with the primary by changing the load seen by the primary. This load variation results in a change in the primary coil current, which is measured and interpreted by a processor in the charging pad. The communication is digital - packets are transferred from the secondary to the primary. Differential Bi-phase encoding is used for the packets. The bit rate is 2Kbits / second.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, power usage packets, end of power packet and efficiency packets.

The primary coil is powered off most of the time. It wakes up occasionally to see if a secondary is present. If a secondary authenticates itself to the primary, the primary remains powered up. The secondary maintains full control over the power transfer using communication packets.

Using the bq5105x as a Wireless Li-Ion/Li-Pol Battery Charger (With reference to Figure 2)

Figure 2 is the schematic of a system which uses the bq5105x as direct battery charger. When the system shown in Figure 2 is placed on the charging pad (transmitter), the receiver coil couples to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C3.

The bq5105x identifies and authenticates itself to the primary using the COM pins by switching on and off the COM FETs and hence switching in and out C_{COMM}. If the authentication is successful, the transmitter will remain powered on. The bq5105x measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$ and sends back error packets to the primary. This process goes on until the RECT voltage settles at $V_{RECT-REG}$.

During power-up, the LDO is held off until the $V_{RECT-REG}$ threshold converges. The voltage control loop ensures that the output (BAT) voltage is maintained at $V_{BAT-REG}$ to power the system depends on the battery charge mode. The bq5105x continues to monitor the V_{RECT} and V_{BAT} and maintains sending error packets to the primary every 250ms. The bq5105x regulates the V_{RECT} voltage very close to battery voltage, this voltage tracking process minimizes the voltage difference across the internal LDO and maximize the charging efficiency. If a large transient occurs, the feedback to the primary speeds up to every 32ms in order to converge on an operating point in less time.

Battery Charge Profile

The bq5105x charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. The charge profile is shown in Figure 18.

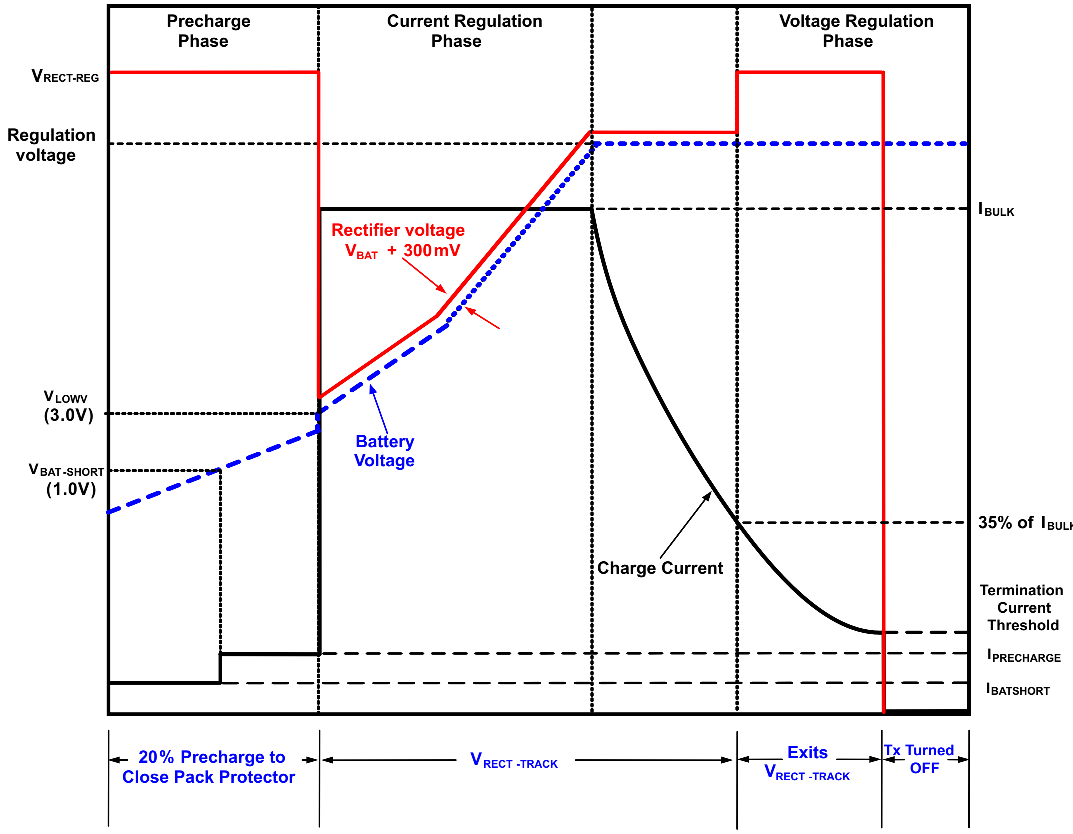


Figure 18. Li-Ion Battery Charger Profile

This allows for proper charge termination and timer operation. Under normal battery charging conditions, the system voltage is approximately equal to the battery voltage, however if the battery is deeply discharged, the system voltage does not drop below 3.5V. This minimum system voltage support enables the system to run with a defective or absent battery pack and enables instant system turn-on even with a totally discharged battery or no battery.

The battery is charged in three phases: precharge, fast-charge constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging. The TS function for bq5105x is JEITA compatible.

Battery Charging Process

Precharge Mode ($V_{BAT} \le V_{LOWV}$)

The bq5105X enters pre-charge mode when $V_{BAT} \le V_{LOWV}$. Upon entering precharge mode, battery charge current limit is set to IPRECHARGE. During pre-charge mode, the charge current is regulated to 20% of the fast charge current (I_{BULK}) setting.

If the battery is deeply discharged or shorted ($V_{BAT} < V_{BAT\text{-}SHORT}$), the bq5105X applies $I_{BAT\text{-}SHORT}$ current to bring the battery voltage up to acceptable charging levels. Once the battery rises above $V_{BAT\text{-}SHORT}$, the charge current is regulated to IPRECHARGE.

Under normal conditions, the time spent in this pre-charge region is a very short percentage of the total charging time and this does not affect the overall charging efficiency for very long.

Fast Charge Mode /Constant Voltage Mode

Once V_{BAT} > V_{LOWV}, the bq5105x enters fast charge mode (Current Regulation Phase) where charge current is regulated using the internal MOSFETs between RECT and BAT.Once the battery voltage charges up to $V_{BAT-REG}$, the bq5105x enters constant voltage (CV) phase and regulates battery voltage to $V_{BAT(REG)}$ and the charging current is reduced.

Once the input current falls below the termination threshold (I_{TERM}),the charger goes into high impedance.

Battery Charge Current Setting Calculations

R_{ILIM} Calculations

The bq5105x includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (e.g., a current compliance). The calculation for the total R_{ILIM} resistance is as follows:

$$R_1 = \frac{300}{I_{BULK}} - R_{FOD} \qquad R_{ILIM} = R_1 + R_{FOD} \tag{1}$$

Where I_{BULK} is the expected maximum battery charge current during fast charge mode and I_{BULK} is the hardware over current limit. When referring to the application diagram shown in Figure 2, R_{ILIM} is the sum of R_{FOD}(188Ω) and the resistance from the I_{LIM} pin to GND).

Termination Calculations

The bq5105X includes a programmable upper termination threshold. This pin can be used to send the charge status 100% packet (CS100) to the transmitter in order to indicate a full charge status. The header for this packet is 0x05. Note that this packet does not turn off the transmitter and is only used as an informative indication of the mobile device's charge status. The upper termination threshold is calculated using Equation 2:

$$R_{TERM} = K_{TERM} \times \%I_{BULK} \tag{2}$$

The K_{TERM} constant is specified in the datasheet as 240. The upper termination threshold is set as a percentage of the ILIM setting.

For example, if the ILIM resistor is set to 300 Ω the ILIM current will be 1A (300 ÷ 300). If the upper termination threshold is desired to be 100 mA, this would be 10% of ILIM. The R_{TERM} resistor would then equal 2.4 kΩ (240 x 10).

Battery-Charger Safety and JEITA Guidelines

The bq5105x continuously monitors battery temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bq5105x compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T4} thresholds. If V_{TS} is outside of this range, the bq5105x suspends charge and waits until the battery temperature is within the V_{T1} to V_{T4} range.

If V_{TS} is within the range of V_{T1} and V_{T2}, the charge current is reduced to I_{BULK}/2. if V_{TS} is within the range of V_{T2} and V_{T3}, the maximum charge voltage regulation is 4.25V. if V_{TS} is within V_{T3} and V_{T4}, the maximum charge voltage regulation is reduced back to 4.10V and charge current is reduced to I_{BULK}/2. Figure 19 summarizes the operation.

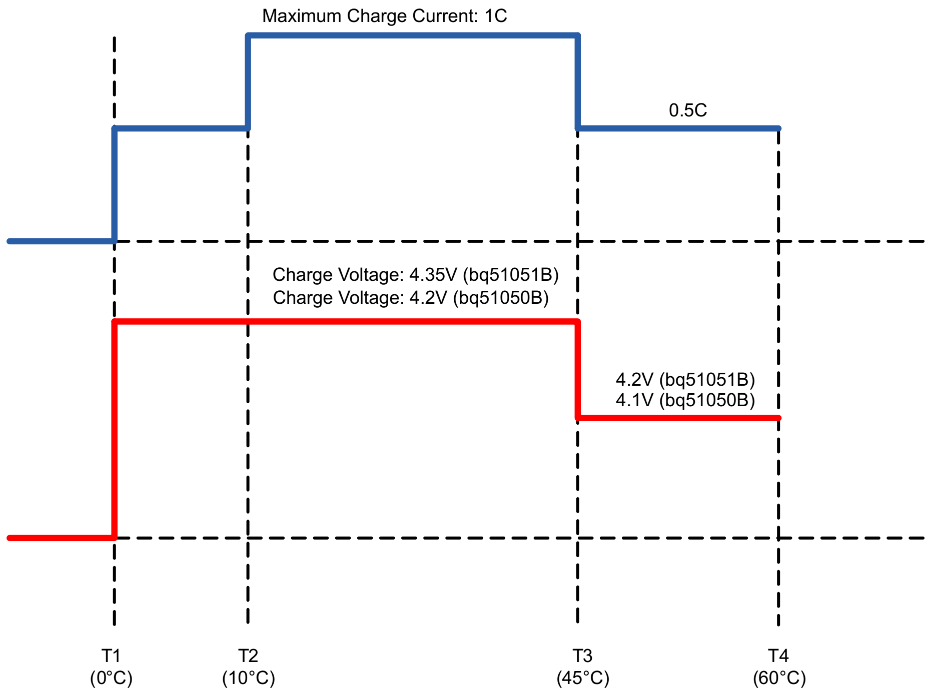


Figure 19. JEITA Compatible TS Profile

Input over-voltage

If, for some condition (e.g., a change in position of the equipment on the charging pad), the rectifier voltage suddenly increases in potential, the voltage-control loop inside the bq5105x becomes active, and prevents the output from going beyond $V_{BAT-REG}$. The receiver then starts sending back error packets every 30ms until the RECT voltage comes back to an acceptable level, and then maintains the error communication every 250ms.

If the input voltage increases in potential beyond V_{OVP}, the IC switches off internal FET and tells the primary to bring the voltage back to $V_{RECT(REG)}$. In additional a proprietary voltage protection circuit is activated by means of C_{clamp1} and C_{clamp2} that protects the IC from voltages beyond the maximum rating of the IC (e.g., 20V).

End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command to terminate power transfer from the TX termed End Power Transfer (EPT) packet. The v1.1 specifies the below reasons and their responding data field value. The *Condition* column corresponds to the case where the bq5101x device will send this command.

REASON	VALUE	CONDITION
Unknown	0x00	AD > 3.6V
Charge Complete	0x01	TS/CTRL = 1
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < 100Ω
Over Temperature	0x03	TS < V_{HOT}, TS > V_{COLD}, or TS/CTRL < 100mV
Over Voltage	0x04	Not Sent
Over Current	0x05	Not Sent
Battery Failure	0x06	Not Sent
Reconfigure	0x07	Not Sent
No Response	0x08	V_{RECT} target does not converge

Status Outputs

The bq5105x provides one status output, $\overline{CHG}$. This output is an open-drain NMOS device that is rated to 20 V. The open-drain FET connected to the $\overline{CHG}$ pin will be turned on whenever the output (BAT) of the chagrer is enabled. As a note, the output of the charger supply will not be enabled if the $V_{RECT(REG)}$ does not converge at the no-load target voltage.

Communication Modulator

The bq5105x provides two identical, integrated communication FETs which are connected to the pins COM1 and COM2. These FETs are used for modulating the secondary load current which allows bq5105x to communicate error control and configuration information to the transmitter. Figure 20 shows how the COMM pins can be used for resistive load modulation. Each COMM pin can handle at most a 24Ω communication resistor. Therefore, if a COMM resistor between 12Ω and 24Ω is required COM1 and COM2 pins must be connected in parallel. bq5105x does not support a COMM resistor less than 12Ω.

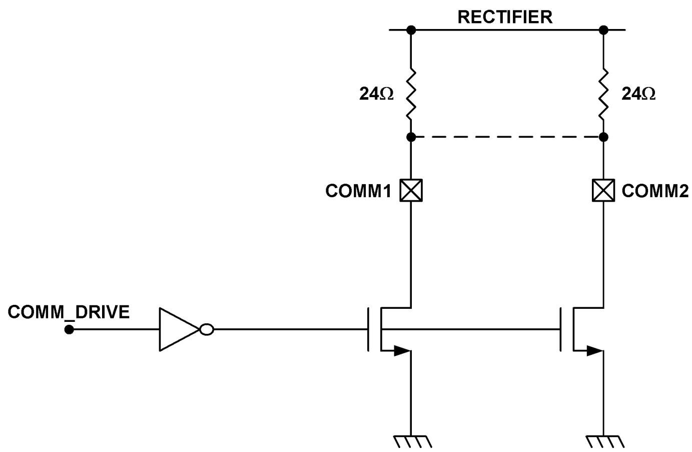


Figure 20. Resistive Load Modulation

In addition to resistive load modulation, the bq5105x is also capable of capacitive load modulation as shown in Figure 21. In this case, a capacitor is connected from COM1 to AC1 and from COM2 to AC2. When the COMM switches are closed there is effectively a 22 nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.

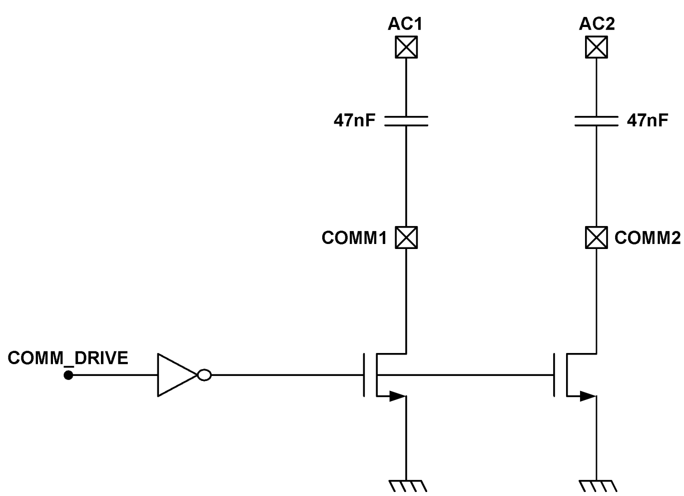


Figure 21. Capacitive Load Modulation

Synchronous Rectification

The bq5105x provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the back gates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial startup of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once VRECT is greater than UVLO, half synchronous mode will be enabled until the load current surpasses 140 mA. Above 140 mA the full synchronous rectifier stays enabled until the load current drops back below 100 mA where half synchronous mode is enabled instead.

Internal Temperature Sense (TS)

The bq5105x includes a ratiometric battery temperature sense circuit. The temperature sense circuit has two ratiometric thresholds which represent a hot and cold condition. An external temperature sensor is recommended to provide safe operating conditions to the receiver product. This pin is best utilized when monitoring the surface that can be exposed to the end user.

The circuit in Figure 22 allows for any NTC resistor to be used with the given V_{HOT} and V_{COLD} thresholds.

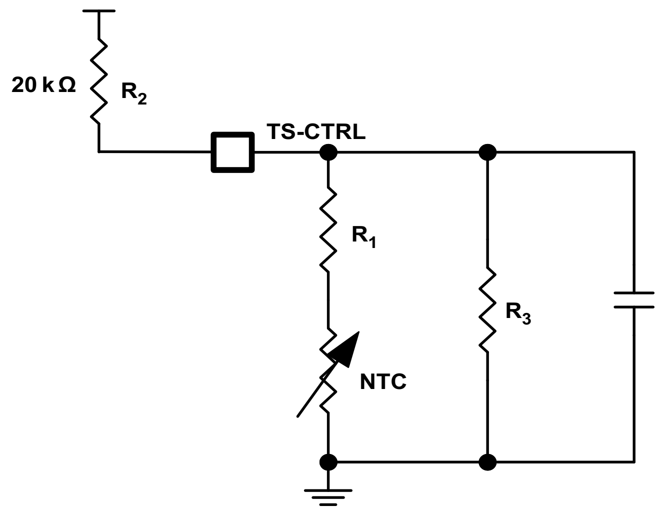


Figure 22. NTC Circuit used for Safe Operation of the Wireless Receiver Power Supply

The resistors R2 and R3 can be solved by resolving the system of equations at the desired temperature thresholds. The two equations are:

$$\%V_{COLD} = \frac{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}}\right)}{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}}\right) + R2} \times 100 \quad (3)$$

$$\%V_{HOT} = \frac{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}}\right)}{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}}\right) + R2} \times 100 \quad (4)$$

Where:

$$R_{NTC}|_{TCOLD} = R_o e^{\beta\left(\frac{1}{TCOLD} - \frac{1}{To}\right)}$$

$$R_{NTC}|_{THOT} = R_o e^{\beta\left(\frac{1}{THOT} - \frac{1}{To}\right)}$$

T_{COLD} and T_{HOT} are the desired temperature thresholds in degrees Kelvin. R_o is the nominal resistance and β is the temperature coefficient of the NTC resistor. An example solution for part number ERT-JZEG103JA is:

R_2 = 7.81 kΩ
R_3 = 13.98 kΩ

Where,

T_{COLD} = 0°C
T_{HOT} = 0°C
β = 4500
R_o = 10 kΩ

The plot of the percent V_{TSB} vs temperature is shown in Figure 23:

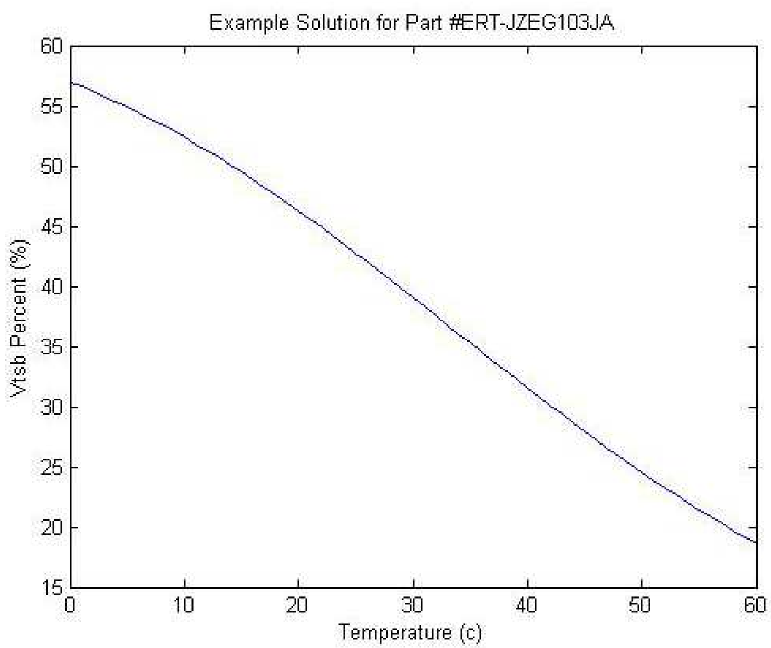


Figure 23. Example Solution for Panasonic Part # ERT-JZEG103JA

Figure 24 illustrates the periodic biasing scheme used for measuring the TS state. The TS_READ signal enables the TS bias voltage for 25 ms. During this period the TS comparators are read (each comparator has a 10 ms deglitch) and appropriate action is taken based on the temperature measurement. After this 25 ms period has elapsed the TS_READ signal goes low, which causes the TS-Bias pin to become high impedance. During the next 100 ms period the TS voltage is monitored and compared to 100 mV. If the TS voltage is greater than 100 mV then a secondary device is driving the TS/CTRL pin and a CTRL = '1' is detected.

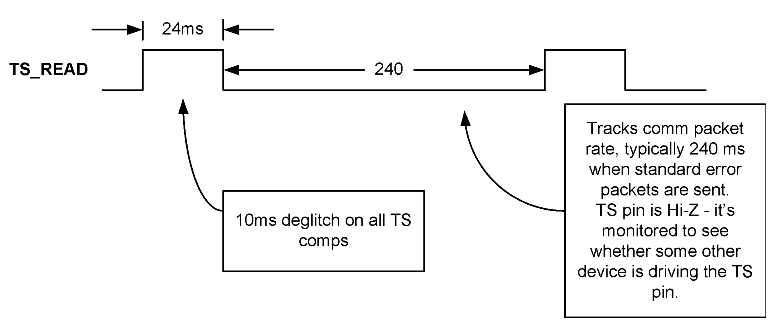


Figure 24. Timing Diagram for TS Detection Circuit

TS/CTRL Function:

The TS-CTRL pin offers three functions:

1. NTC temperature monitoring,
2. Charge done indication,
3. Fault indication

When NTC is connected between TS/CTRL pin and the GND, the NTC is function is allowed to operate. If the TS/CTRL pin is pulled to the battery voltage, the Rx is shutdown with the indication of a charge complete condition. If the TS-CTRL pin is pulled to GND, The Rx is shutdown with the indication of a fault.

Thermal Protection

The bq5105x includes a thermal shutdown protection. If the die temperature reaches TJ(OFF), the LDO is shut off to prevent any further power dissipation.

WPC 1.1 Compatibility

The bq5105x is a WPC 1.1 compatible device, In order to enable a Power Transmitter to monitor the power loss across the interface as one of the possible methods to limit the temperature rise of Foreign Objects, the bq51050B reports its Received Power to the Power Transmitter. The Received Power equals the power that is available from the output of the Power Receiver plus any power that is lost in producing that output power. For example, the power loss includes (but is not limited to) the power loss in the Secondary Coil and series resonant capacitor, the power loss in the Shielding of the Power Receiver, the power loss in the rectifier, the power loss in any post-regulation stage, and the eddy current loss in metal components or contacts within the Power Receiver. In WPC1.1 specification, foreign object detection (FOD) is enforced, that means the bq51050B will send received power information with known accuracy to the transmitter.

WPC 1.1 defines Received Power is “the average amount of power that the Power Receiver receives through its Interface Surface, in the time window indicated in the Configuration Packet”.

A Receiver will be certified as WPC 1.1 only after meeting following requirement The DUT (Device Under Test) is tested on a Reference Transmitter whose transmitted power is calibrated, the receiver must send a received power such that:

0 < (TX PWR) REF – (RX PWR out) DUT < 250mW

This 250mW bias ensures that system will remain interoperable.

WPC 1.1 Transmitter will be tested to see if they can detect reference Foreign Objects with a Reference receiver. WPC1.1 Specification will allow much more accurate sensing of Foreign Objects.

A Transmitter can be certified as a WPC 1.1 only after meeting the following requirement- A Transmitter is tested to see if it can prevent some reference Foreign Objects (disc, coin, foil) from exceeding their threshold temperature (60°C, 80°C).

Series and Parallel Resonant Capacitor Selection

Shown in Figure 2, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.1 specification. Figure 25 illustrates the equivalent circuit of the dual resonant circuit:

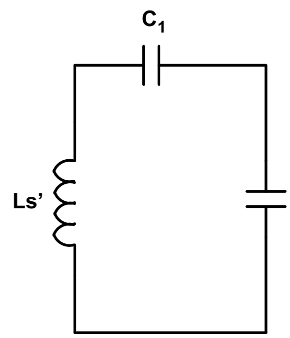


Figure 25. Dual Resonant Circuit with the Receiver Coil

Section 4.2 (Power Receiver Design Requirements) in volume 1 of the WPC v1.1 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required take inductance measurements with a fixed test fixture. The test fixture is shown in Figure 26:

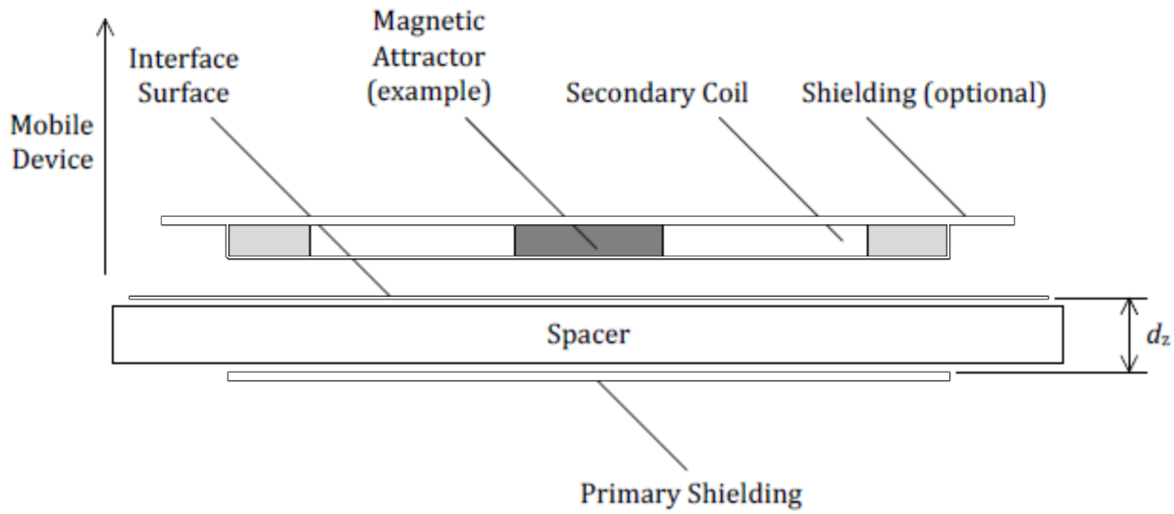


Figure 26. WPC v1.1 Receiver Coil Test Fixture for the Inductance Measurement Ls'

The primary shield is to be 50 mm x 50 mm x 1 mm of Ferrite material PC44 from TDK Corp. The gap dZ is to be 3.4 mm. The receiver coil, as it will be placed in the final system (e.g. the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. This measurement is termed Ls or the free-space inductance. Each capacitor can then be calculated using Equation 5:

$$C_1 = \frac{1}{(2\pi \times f\text{s})^2 \times L'_s}$$

$$C_2 = \frac{1}{(2\pi \times f_D)^2 \times \left(L_s - \frac{1}{C_1}\right)} \quad (5)$$

Where f_S is 100 kHz +5/–10% and f_D is 1 MHz ±10%. C1 must be chosen first prior to calculating C2. The quality factor must be greater than 77 and can be determined by Equation 6:

$$Q = \frac{2\pi \times f_D \times Ls}{R} \quad (6)$$

Where R is the DC resistance of the receiver coil. All other constants are defined above.

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ51050BRHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ51050B	Samples
BQ51050BRHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ51050B	Samples
BQ51050BYFPR	ACTIVE	DSBGA	YFP	28	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		BQ51050B	Samples
BQ51050BYFPT	ACTIVE	DSBGA	YFP	28	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		BQ51050B	Samples
BQ51051BRHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ51051B	Samples
BQ51051BRHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ51051B	Samples
BQ51051BYFPR	ACTIVE	DSBGA	YFP	28	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		BQ51051B	Samples
BQ51051BYFPT	ACTIVE	DSBGA	YFP	28	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		BQ51051B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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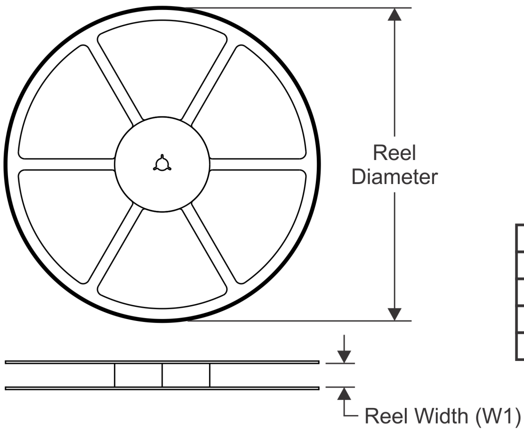
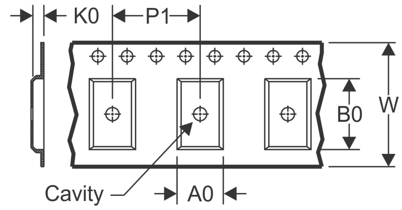
TAPE AND REEL INFORMATION

REEL DIMENSIONS

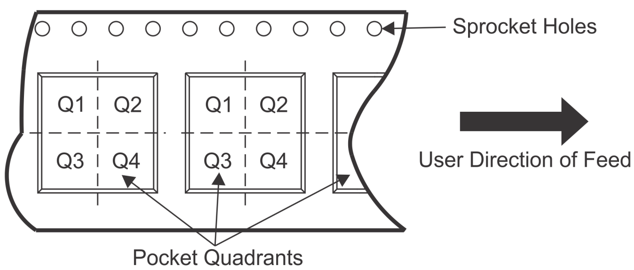


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

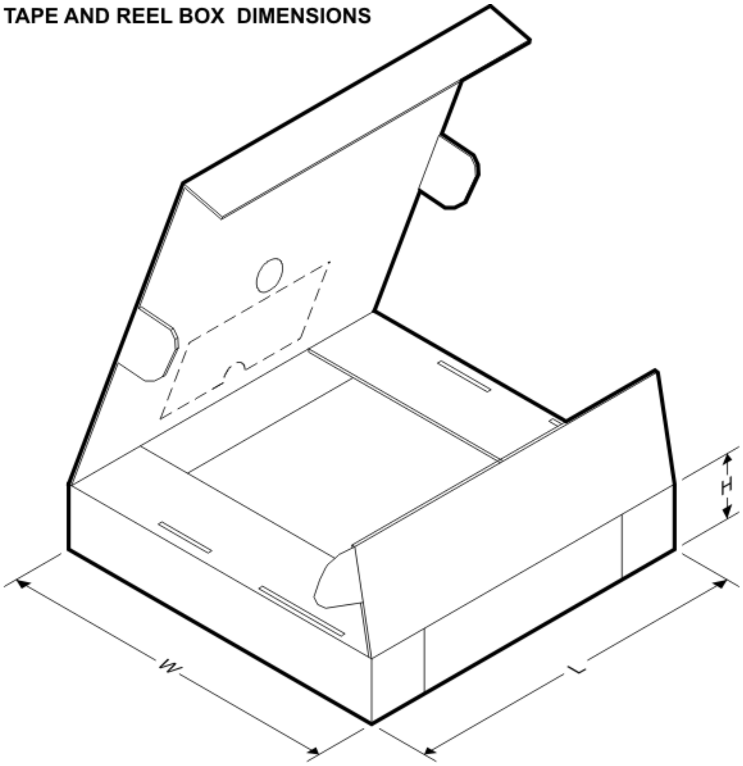
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51050BRHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51050BRHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51050BYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51050BYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51051BRHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51051BRHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51051BYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51051BYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1

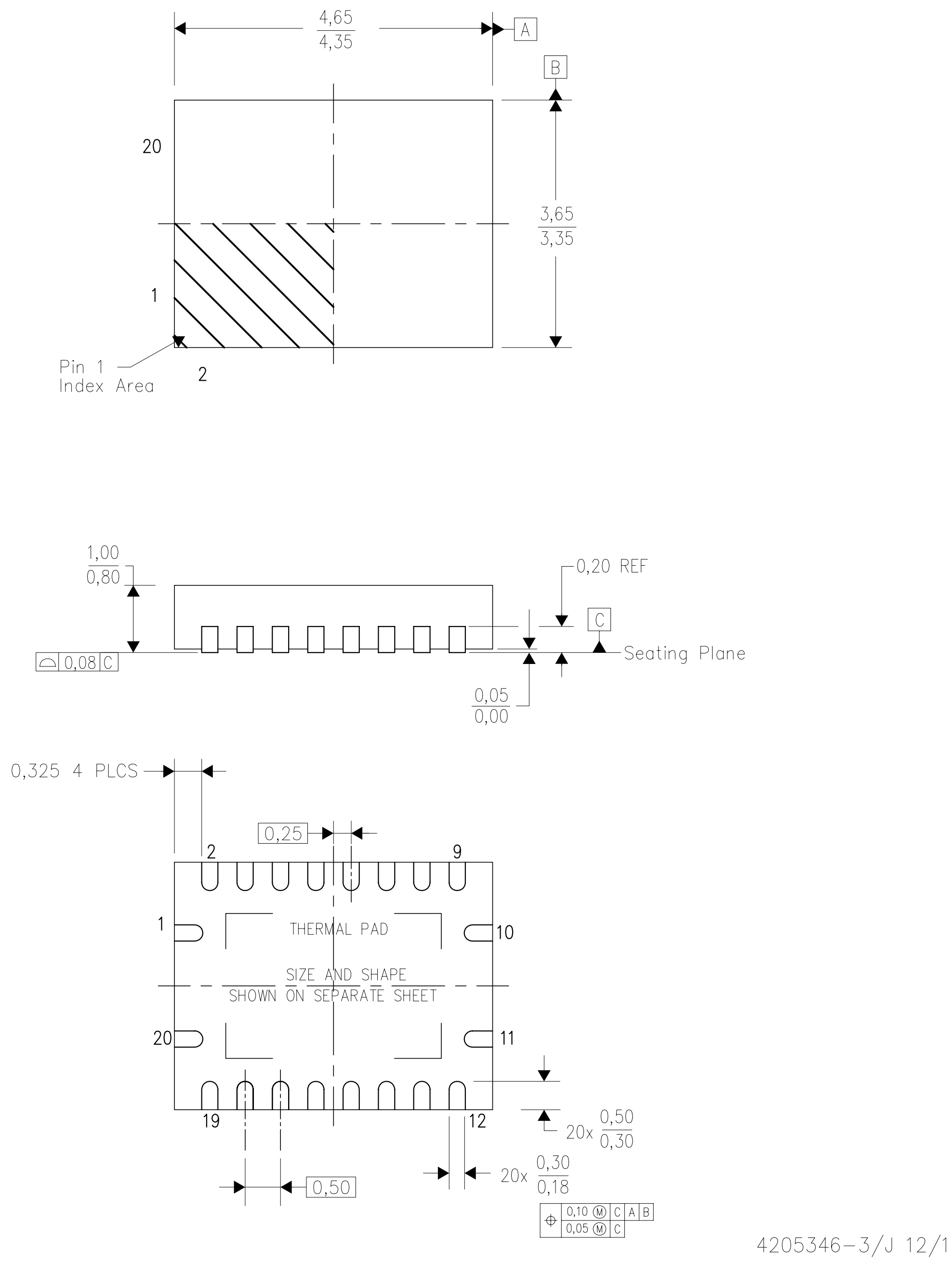
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51050BRHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ51050BRHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51050BYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51050BYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0
BQ51051BRHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ51051BRHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51051BYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51051BYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0

RHL (R-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

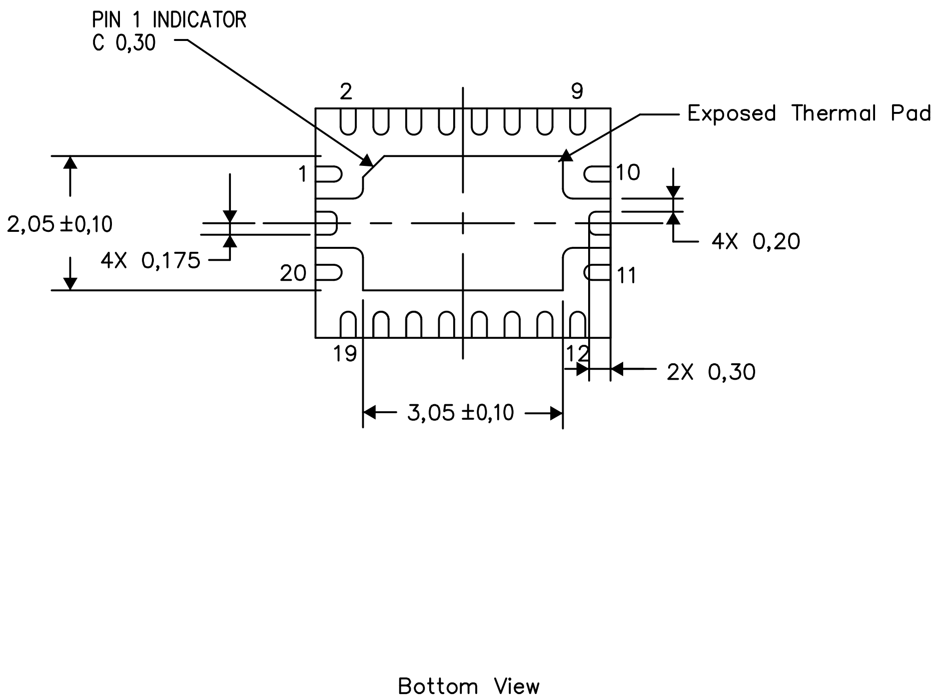
RHL (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

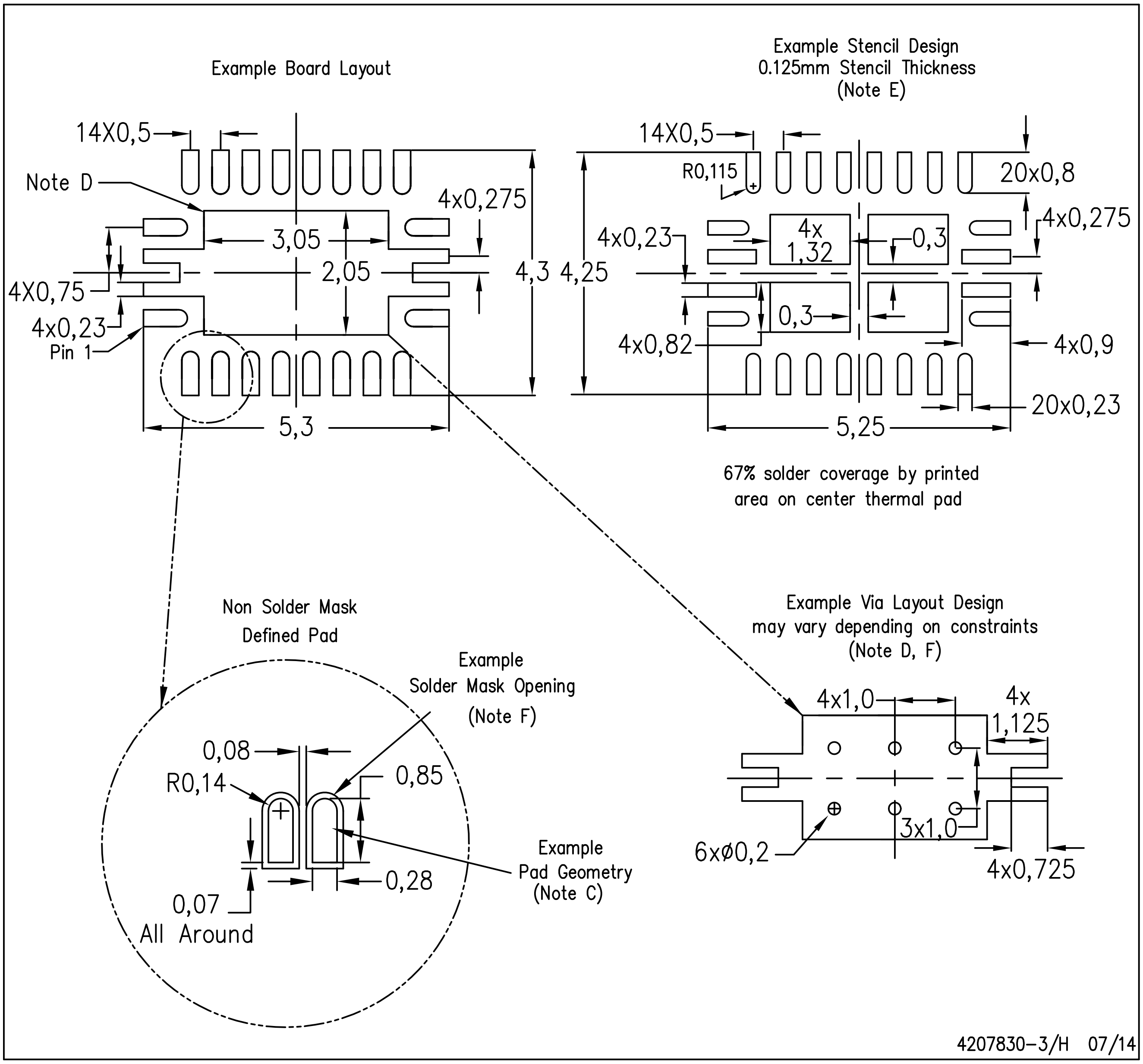


Exposed Thermal Pad Dimensions

4206363-3/N 07/14

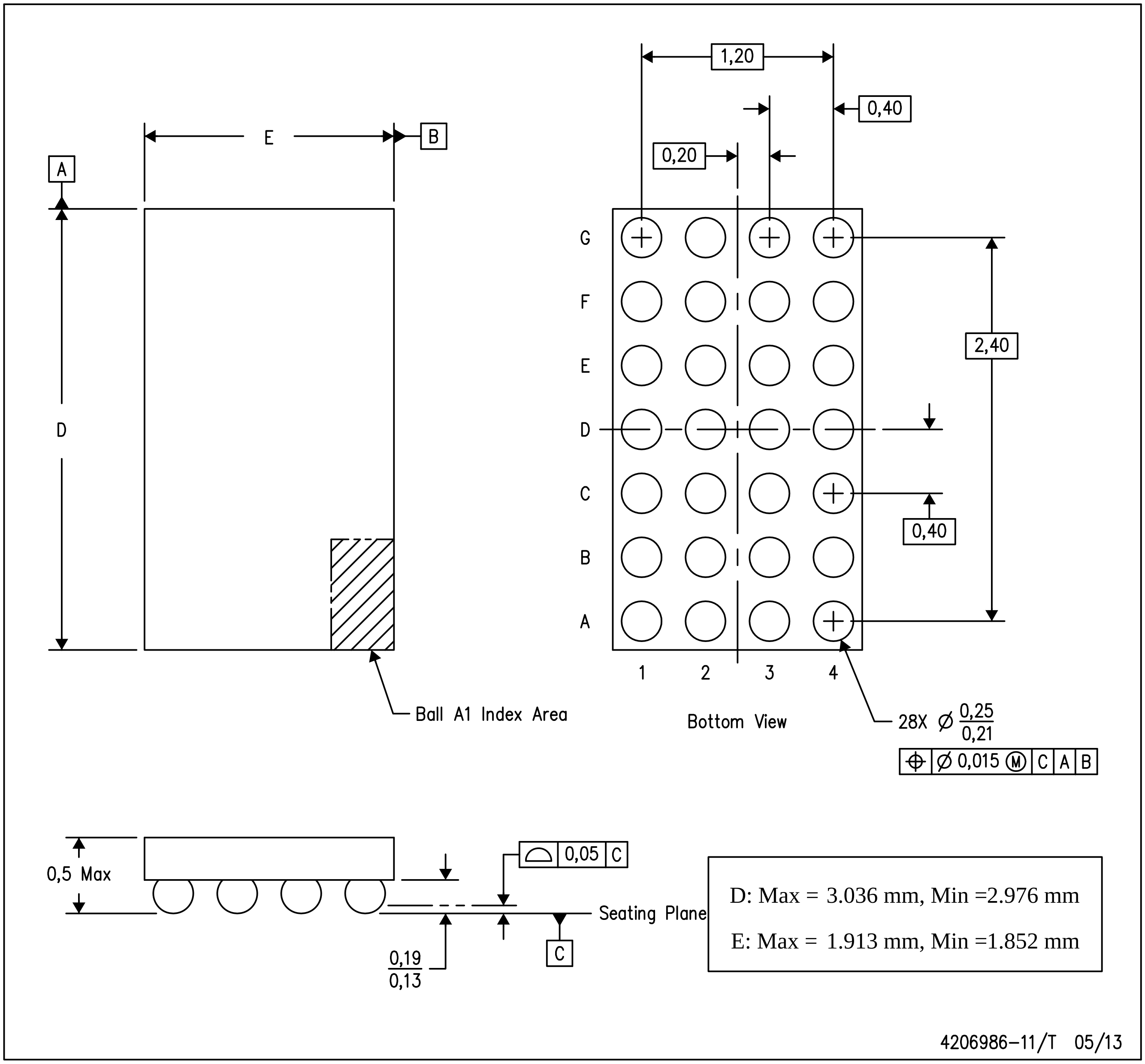
NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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