

Quick Start Guide for testing the AD9213 ADC Evaluation Board using the ADS8-V1EBZ FPGA based Capture Board

TYPICAL SETUP



Figure 1. AD9213 Evaluation Board and ADS8-V1EBZ Data Capture Board

EQUIPMENT NEEDED

- Signal Generators:
 - Analog signal source: The frequency and power requirements depend on the tests to be performed. A bandpass filter is often used for single tone tests.
 - Analog Clock source: The clock signal generator should have very low phase noise, and be capable of supplying a 10GHz clock signal (or 6GHz clock signal for the 6Gbps speed grade of AD9213) at about 10dBm.
 - Reference clock source: For AD9213-10GBZ with 16 output lanes, at 10Gbps, the frequency of REFCLK is 625MHz. For AD9213-6GBZ configured for 8 output lanes, at 6Gbps, the frequency of REFCLK is 750MHz. For AD9213 the frequency of REFCLK is the digital output lane rate divided by 20.
- PC running Windows
- USB port and cable to connect to PC
- AD9213 Evaluation Board
- AD9213 Regulator Board (supplies power to the ADC board)
- ADS8-V1EBZ FPGA Based Data Capture Board, with power supply

HELPFUL DOCUMENTS

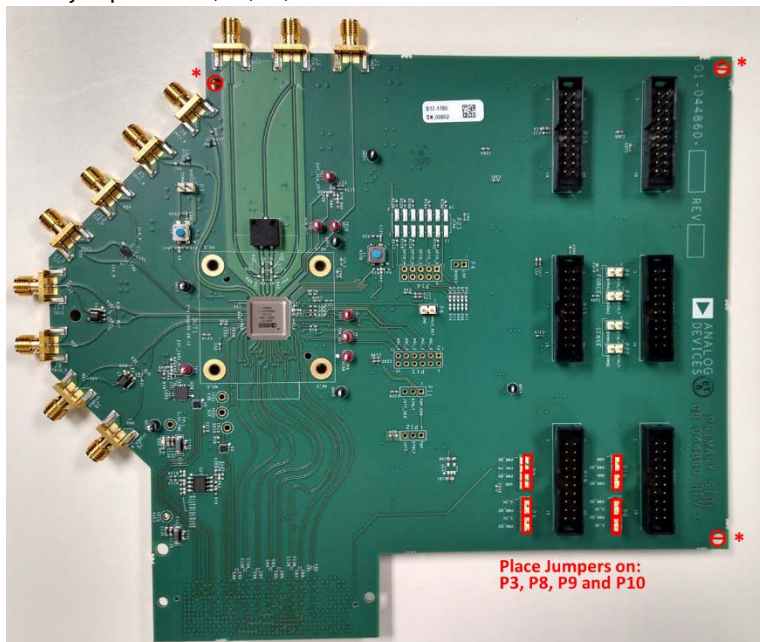
- AD9213 Preliminary Datasheet
- ACE Manual: http://swdownloads.analog.com/ACE/ACE_User_Manual_rev3.pdf

SOFTWARE NEEDED

- Analysis Control Evaluation (ACE) software: available at <http://www.analog.com/en/design-center/evaluation-hardware-and-software/ace-software.html>
- AD9213 ACE Plugin: Analog Devices will supply this.

TESTING

1. Install Analysis | Control | Evaluation (ACE) Software. The installer is located at <http://www.analog.com/en/design-center/evaluation-hardware-and-software/ace-software.html>.
2. After ACE is installed, locate the AD9213 plugin installer (provided separately by email, flash-drive, or other media). Double-click on this executable. It will automatically install the AD9213 ACE plugin. Perform this step without the board connected to the PC.
3. Close ACE.
4. Install jumpers on P3, P8, P9, P10 as shown.

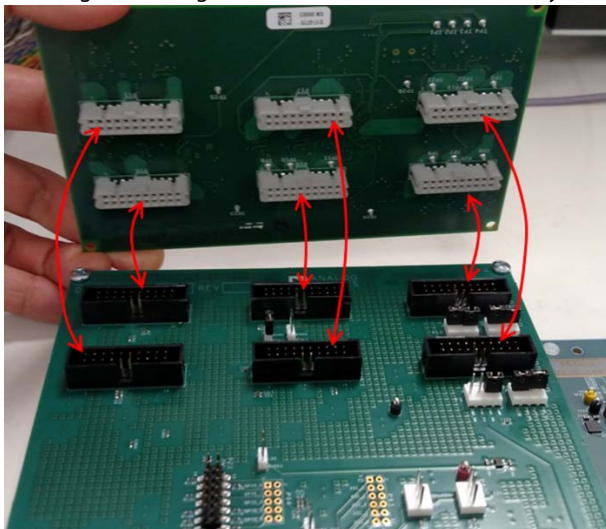


*Standoff and Screw locations



Standoffs can be installed at the *locations if desired. Alternatively, foam sheets can be used to support the board.

5. Connect the AD9213 evaluation board to the regulator board. The connectors mate as shown. With the boards parallel to each other, carefully align the connectors, then press the boards together applying even pressure over the connectors to avoid stressing and flexing the boards. The connectors are keyed so it is impossible to insert the board with the incorrect orientation.

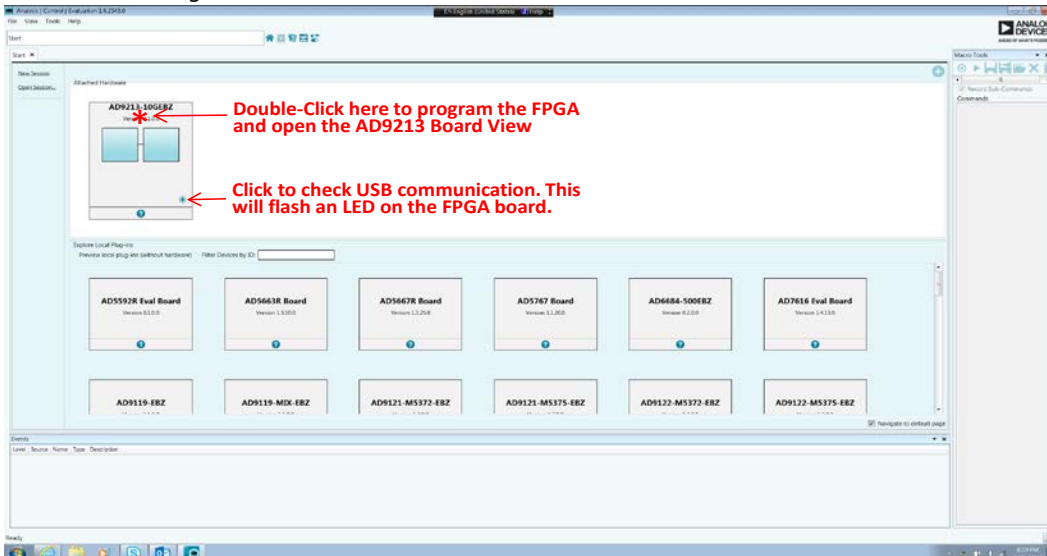


6. Connect the AD9213 evaluation board/regulator board combo to the ADS8-V1EBZ board together as shown in Figure 1. Align the FMC+ connectors and apply even pressure across the connector and press the FMC connector on to its counterpart on the FPGA board.
7. Connect signal, clocks, power and USB cables to the boards as shown in Figure 1.
 - a. Signal (J3): The frequency and amplitude of the test signal depend on the type of test being performed. Full scale is typically achieved at 9dBm – 12dBm signal power at the signal generator, depending on frequency. If in doubt about what amplitude to use, start with a lower amplitude (e.g. 4dBm at the signal generator) and work up or down from there.
 - i. *Note: In Figure 1 the input signal is shown being applied to RF connector J3. As can be seen, the trace from J3 goes to the balun, where the single ended signal is converted to differential. On some board revisions the trace to the balun comes from RF connector J2. In those cases the input signal must be applied to J2.



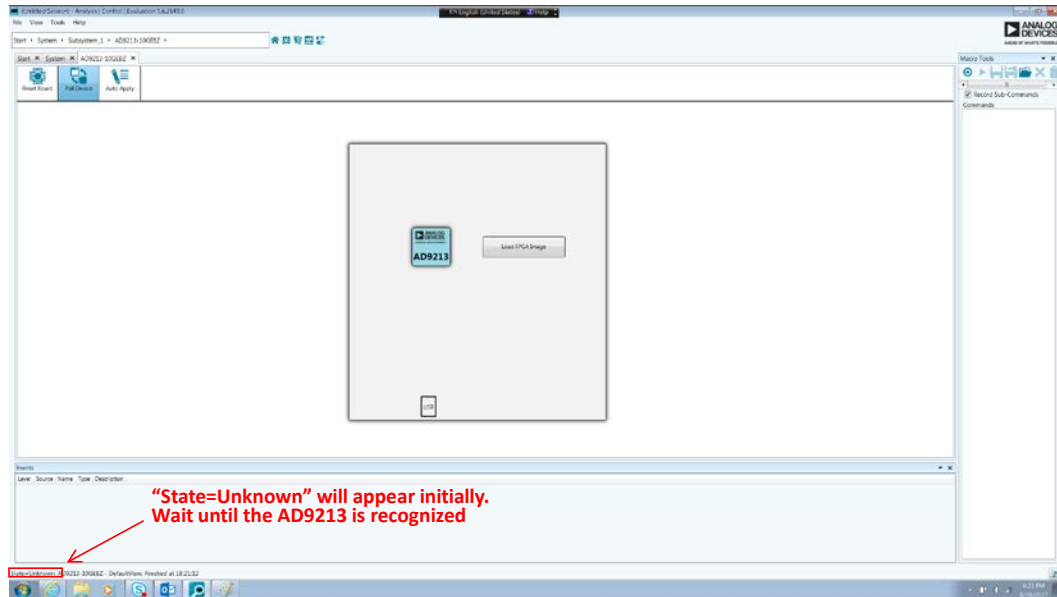
- b. Sample clock (J13): The sample clock works well across a wide range of amplitudes (1dBm – 10dBm at the signal generator). Because jitter performance is likely to improve as the slew rate increases, choose an amplitude towards the upper end of the stated range.
 - c. Reference Clock (ADS8-V1EBZ AJ1): Like the sample clock, the reference clock works well across a wide range of amplitudes (1dBm – 10dBm at the signal generator). Unlike the sample clock, the reference clock is not sensitive to jitter/phase noise. Any signal generator that meets the frequency and power requirements will work. For AD9213 the frequency of the reference clock is the (output digital data rate)/20.
 - i. Example: For the default JESD204B output configuration of AD9213-10GEBZ (L = 16, N' = 16, M = 1) at 10Gbps, the output data rate is 12.5Gbps. Reference clock frequency = 12.5G/20 = 625MHz.
 - ii. Example: For AD9213-6GEBZ, ACE brings the part up in 8-Lane mode. In this case (L = 8, N' = 16, M = 1) at 6Gbps, the output data rate is 15Gbps. Reference clock frequency = 15G/20 = 750MHz.
 - d. Connect the USB cable from the ADS8-V1EBZ FPGA board to the Windows PC that has ACE installed.
8. Turn on the signal generators for clock, reference clock, and signal.
9. Power on the ADS8-V1EBZ FPGA board using the switch S4. Wait several seconds after powering on the ADS8-V1EBZ, until DS17 flashes and the FPGA fan has stopped spinning.

10. Start ACE. You will get a screen that looks similar to this:



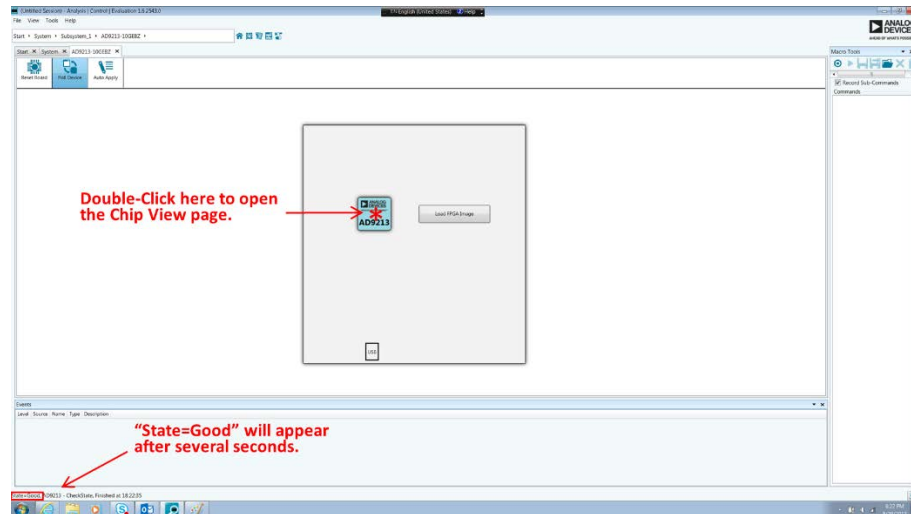
Double-Click the “AD9213-10GEBZ” or “AD9213-6GEBZ” icon.

11. This is the AD9213 board view.



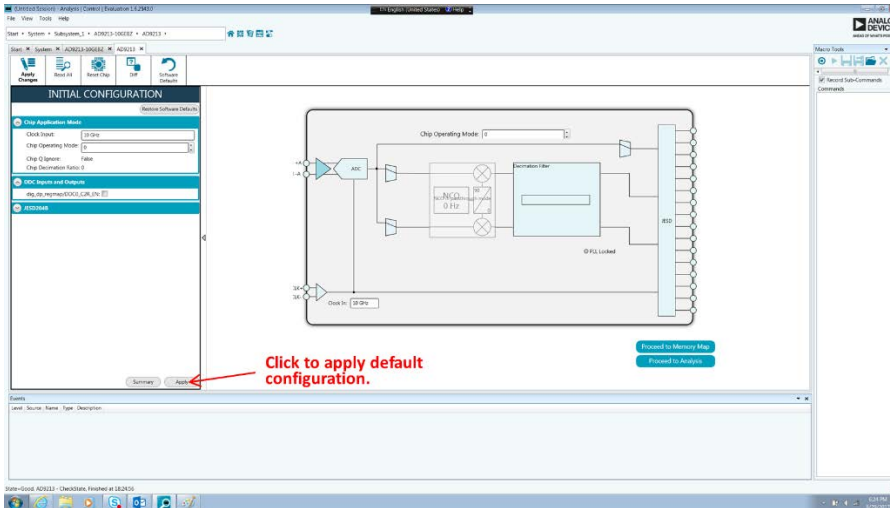
“Unknown” will initially appear in the lower left corner. Wait until “Unknown” changes to “Good”.

12. AD9213 board view with “State=Good”

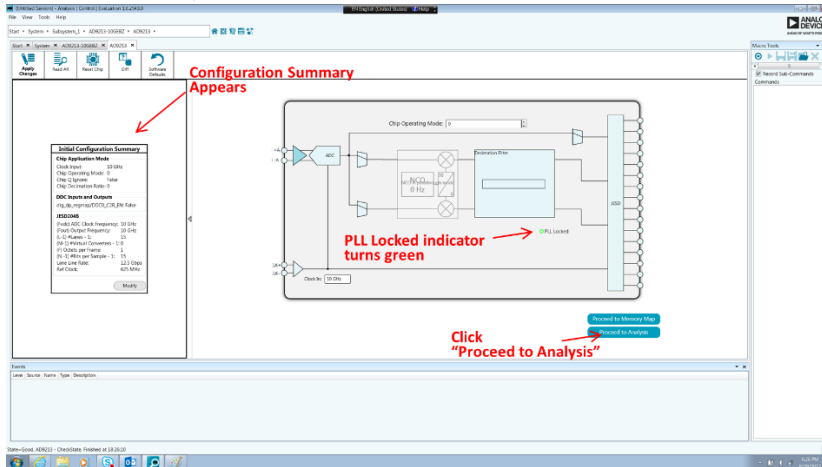


Double-Click the AD9213 icon after “State=Good” appears in the lower left. This will bring up the Chip View.

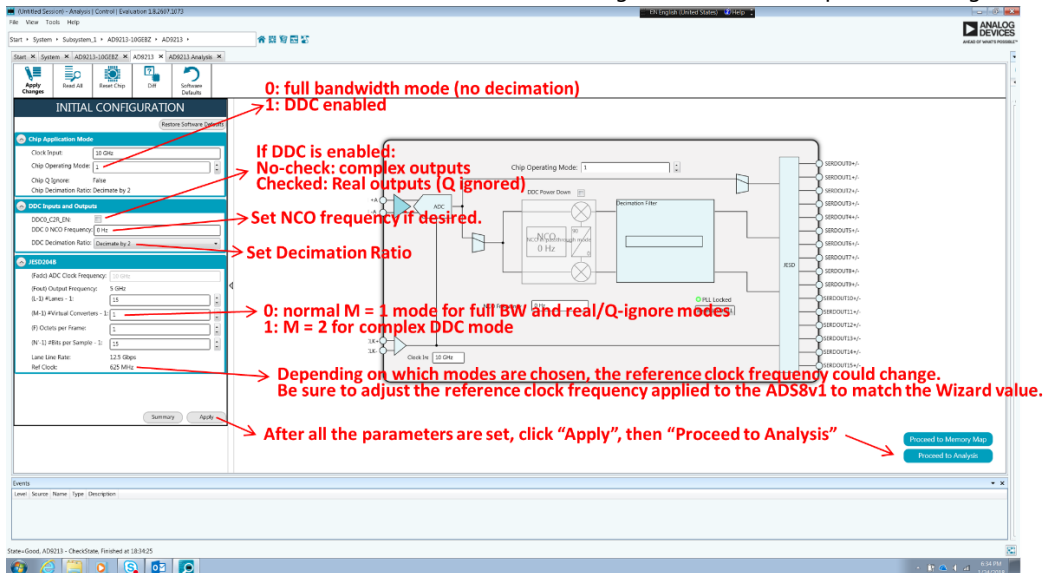
13. AD9213 Chip View



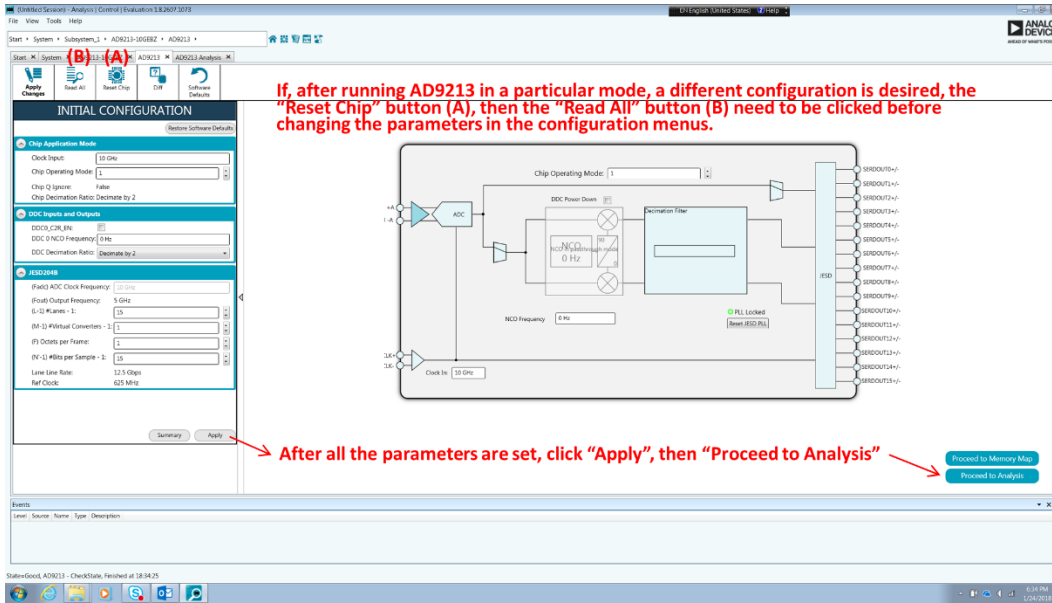
Click the Apply button to configure AD9213 in its **default** configuration. The window will then look something like this:



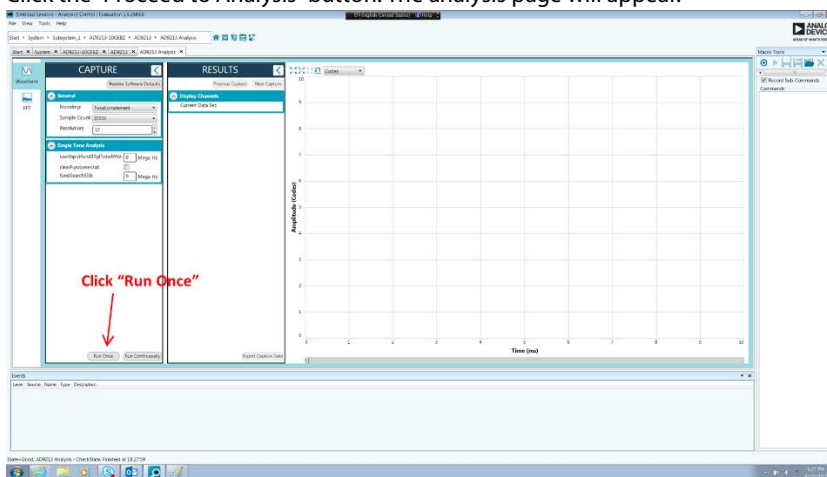
AD9213 DDC and NCO controls have been added to the configuration Wizard. The picture below gives a summary of the settings.



The settings above work if you are starting ACE after initial board power-up and are setting the DDC and NCO as the initial configuration to be evaluated. If you already have AD9213 up-and-running, and would like to go back and change the DDC and/or NCO configuration, you must first click the Reset Chip button, and then the Read All button as shown below.

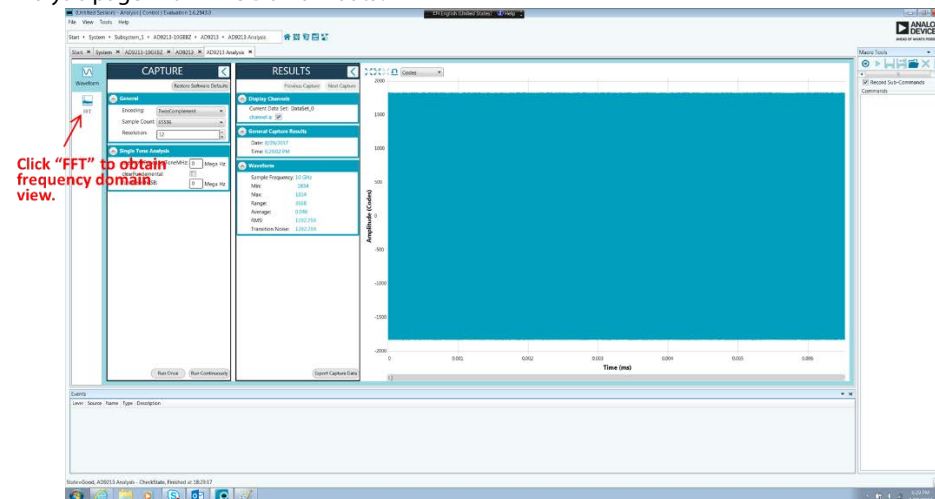


14. Click the "Proceed to Analysis" button. The analysis page will appear.



Click "Run Once" to get a time domain look at the converted data.

15. Analysis page with Time Domain data:



Click on the "FFT" icon to see the frequency domain view (FFT).

