Document Number: A2V07H525-04N
Rev. 0, 07/2017

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 120 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 595 to 851 MHz.

600 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.5 Vdc, P_{out} = 120 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
595 MHz	17.8	54.7	6.8	–27.5
623 MHz	17.5	56.9	7.2	–29.2
652 MHz	17.3	53.4	6.8	–27.2

780 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 1.25 Vdc, P_{out} = 120 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

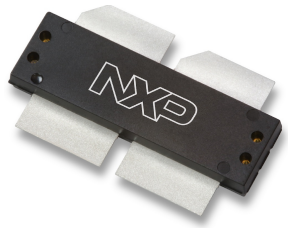
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
758 MHz	18.4	53.0	7.1	–31.1
780 MHz	18.3	54.1	7.1	–31.1
803 MHz	17.5	54.1	6.7	–30.6

Features

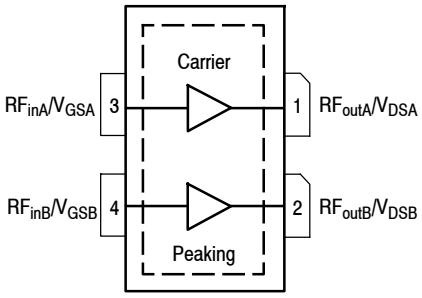
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2V07H525-04NR6

**595–851 MHz, 120 W AVG., 48 V
AIRFAST RF POWER LDMOS
TRANSISTOR**



**OM-1230-4L
PLASTIC**



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 120 W Avg., W-CDMA, 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.5 Vdc, 623 MHz	$R_{\theta JC}$	0.37	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 700 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.0	2.5	3.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.21	0.5	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 280 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.8 Adc)	$V_{DS(on)}$	0.1	0.21	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

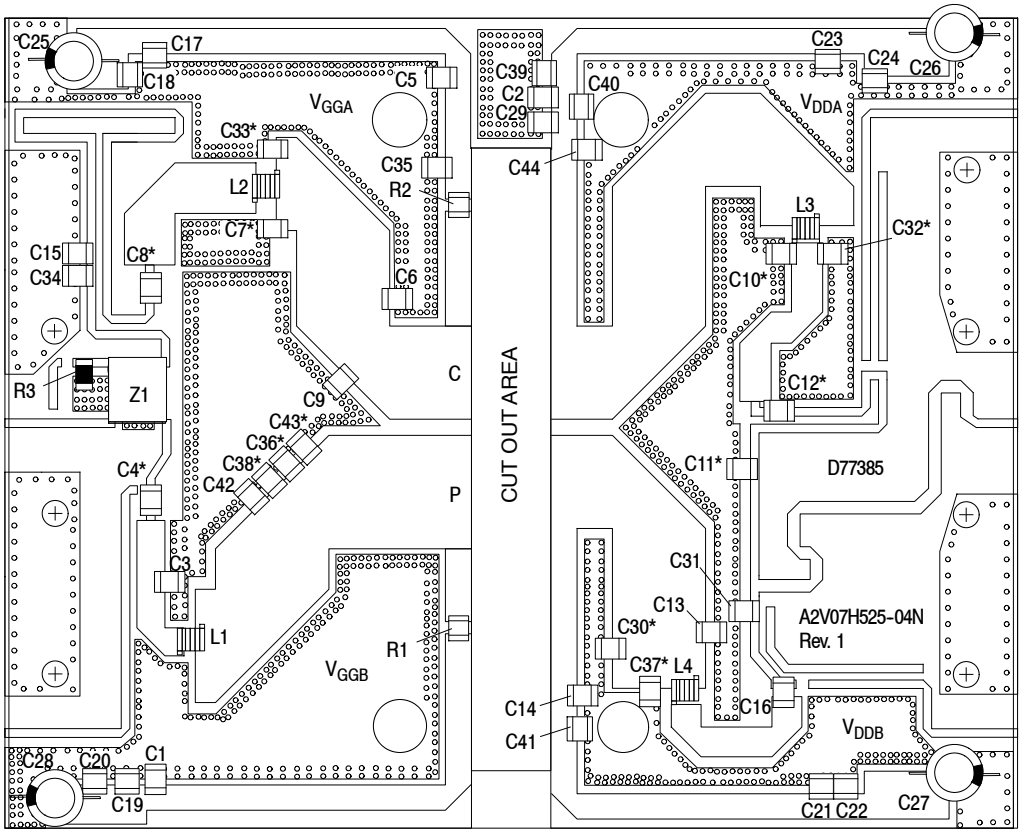
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.5 Vdc, P_{out} = 120 W Avg., f = 623 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.8	17.5	20.0	dB
Drain Efficiency	η_D	54.2	56.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.5	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	–29.2	–27.0	dBc
Load Mismatch (2) (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 700 mA, V_{GSB} = 0.5 Vdc, f = 623 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 55 Vdc, 363 W Pulsed CW Output Power (3 dB Input Overdrive from 182 W Pulsed CW Rated Power)		No Device Degradation			
Typical Performance (2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.5 Vdc, 595–652 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (3)	P3dB	—	602	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 595–652 MHz frequency range)	Φ	—	–18	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 57 MHz Bandwidth @ P_{out} = 120 W Avg.	G_F	—	0.6	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.005	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2V07H525-04NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L

1. Part internally input matched.
2. Measurement made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C4, C7, C8, C10, C11, C12, C30, C32, C33, C36, C37, C38 and C43 are mounted vertically.

Figure 2. A2V07H525-04NR6 Test Circuit Component Layout

Table 7. A2V07H525-04NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C5, C8	240 pF Chip Capacitor	ATC100B241JT200XT	ATC
C2, C14, C29, C40	300 pF Chip Capacitor	ATC100B301JT200XT	ATC
C3, C42	6.8 pF Chip Capacitor	ATC100B5R0BT500XT	ATC
C4	470 pF Chip Capacitor	ATC100B471JT200XT	ATC
C6	18 pF Chip Capacitor	ATC100B180JT500XT	ATC
C7, C43	8.2 pF Chip Capacitor	ATC100B8R2BT500XT	ATC
C9, C36	5.6 pF Chip Capacitor	ATC100B5R6BT500XT	ATC
C10, C32	1 pF Chip Capacitor	ATC800B1R0BT500XT	ATC
C11	5.1 pF Chip Capacitor	ATC100B5R1BT500XT	ATC
C12, C35	120 pF Chip Capacitor	ATC100B121JT200XT	ATC
C13	16 pF Chip Capacitor	ATC100B160JT500XT	ATC
C15, C38	3.6 pF Chip Capacitor	ATC100B3R6BT500XT	ATC
C16	180 pF Chip Capacitor	ATC100B181JT200XT	ATC
C17, C18, C19, C20, C21, C22, C23, C24, C39, C41, C44	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
C25, C26, C27, C28	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C30, C37	6.8 pF Chip Capacitor	ATC100B6R8BT500XT	ATC
C31	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C33, C34	2 pF Chip Capacitor	ATC100B2R0BT500XT	ATC
L1, L2, L3, L4	2.5 nH Inductor, 1 Turn	A01TKLC	Coilcraft
R1, R2	2.2 Ω Chip Resistor	CRCW12062R20JNEA	Vishay
R3	50 Ω, 4 W Termination Chip Resistor	CW12010T0050GBK	ATC
Z1	560–680 MHz Band, 90°, 3 dB Hybrid Coupler	GSC267-HYB0620	Soshin
PCB	Rogers RO4360G2, 0.020″, ε_r = 6.4	D77385	MTL

TYPICAL CHARACTERISTICS — 595–652 MHz

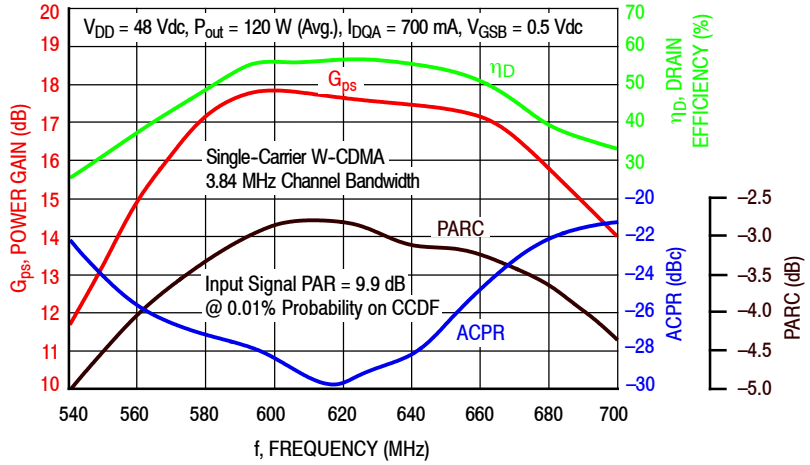


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 120 Watts Avg.

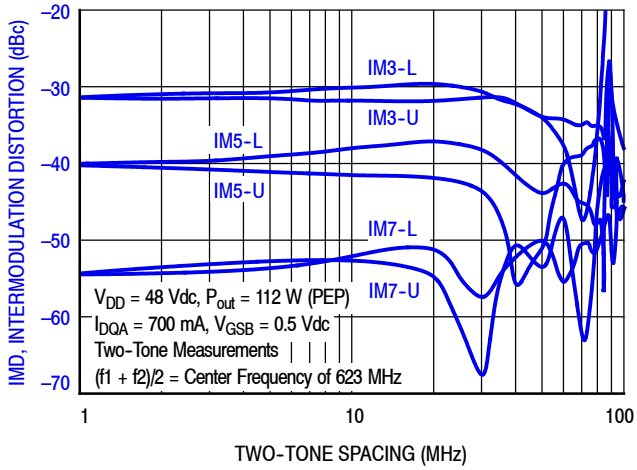


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

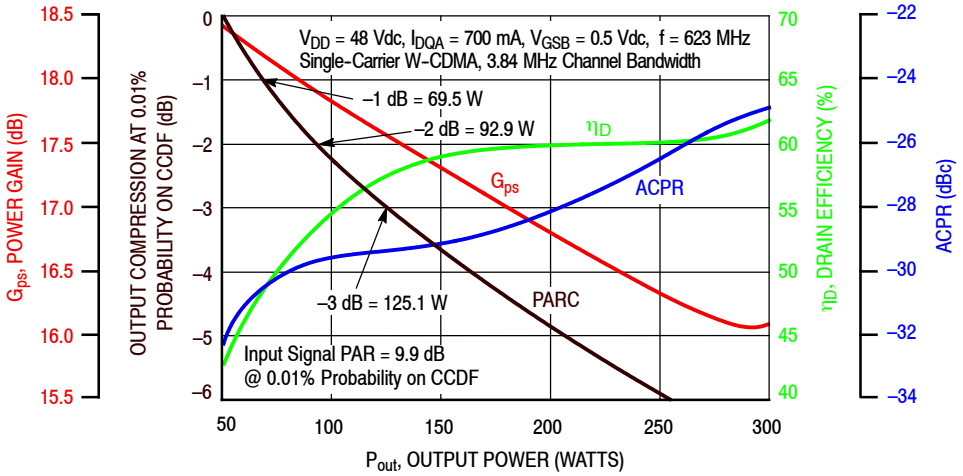


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 595–652 MHz

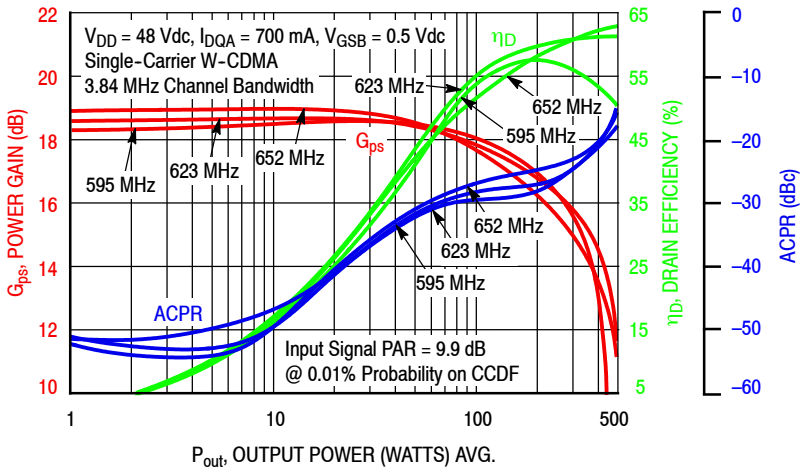


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

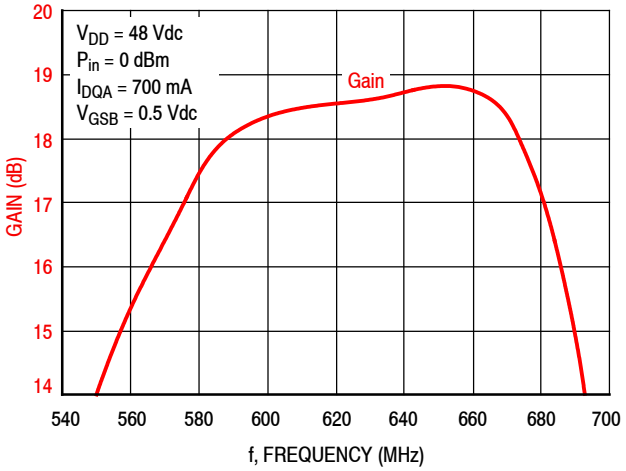


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 701 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.07 – j0.52	5.37 + j0.48	2.93 + j0.08	20.5	54.0	250	58.2	–10
652	4.10 – j1.84	3.77 + j2.27	2.99 + j0.54	21.1	54.2	262	63.0	–9

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.07 – j0.52	5.12 + j0.52	2.88 – j0.02	18.3	54.6	286	58.2	–12
652	4.10 – j1.84	3.59 + j2.50	3.33 + j0.69	19.3	54.7	293	66.7	–11

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 701 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.07 – j0.52	4.31 + j0.61	3.20 + j3.58	23.5	51.2	131	68.8	–14
652	4.10 – j1.84	2.83 + j2.71	2.12 + j4.47	24.4	50.1	102	78.1	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.07 – j0.52	4.52 + j0.59	3.30 + j2.55	20.8	52.9	196	67.5	–16
652	4.10 – j1.84	3.16 + j2.88	3.15 + j3.42	21.3	52.9	196	78.8	–17

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

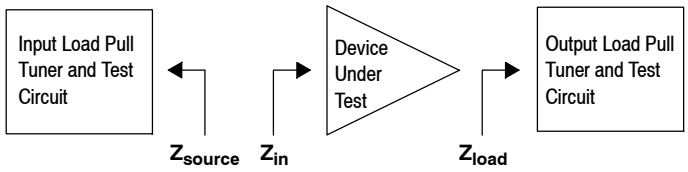


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	2.46 – j0.30	2.82 + j0.31	1.39 + j0.02	15.9	57.1	518	64.0	–20
652	1.67 – j1.64	1.96 + j1.37	1.36 – j0.12	15.5	57.2	529	62.8	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	2.46 – j0.30	2.61 + j0.36	1.42 – j0.03	13.8	57.7	595	64.1	–22
652	1.67 – j1.64	1.81 + j1.47	1.47 – j0.17	13.5	57.9	611	65.4	–22

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

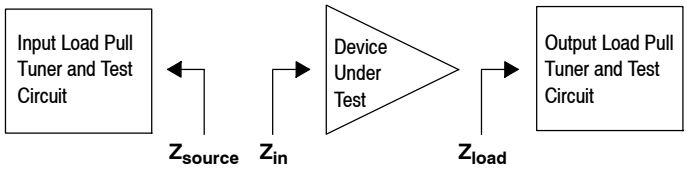
Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	2.46 – j0.30	2.62 + j0.10	1.27 + j2.08	16.3	53.5	221	81.4	–32
652	1.67 – j1.64	1.82 + j1.34	1.84 + j1.64	16.3	55.1	321	80.2	–24

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	2.46 – j0.30	2.49 + j0.23	1.40 + j1.66	14.6	55.1	325	77.7	–36
652	1.67 – j1.64	1.71 + j1.44	1.87 + j1.54	14.3	55.8	381	80.5	–28

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 652 MHz

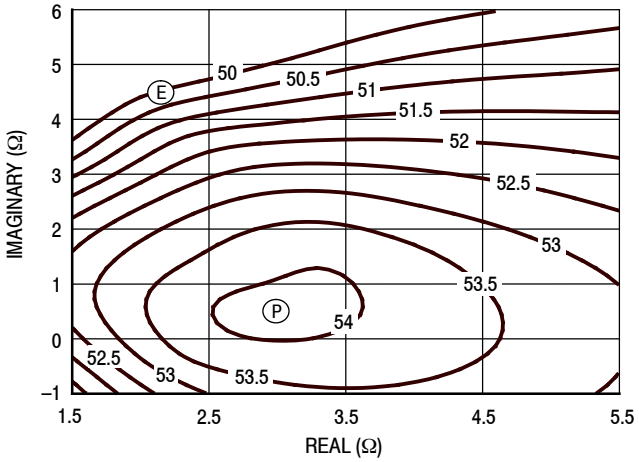


Figure 8. P1dB Load Pull Output Power Contours (dBm)

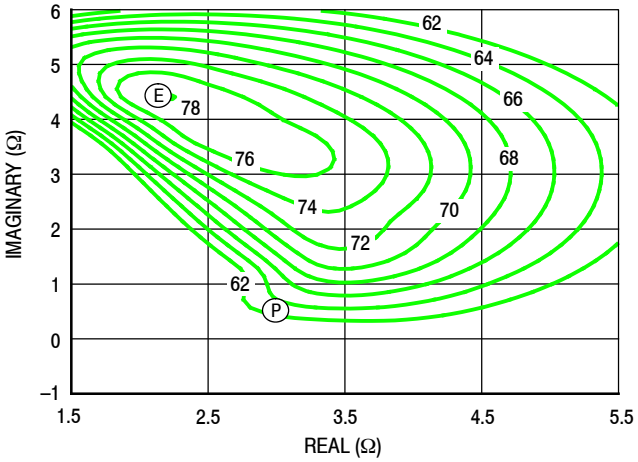


Figure 9. P1dB Load Pull Efficiency Contours (%)

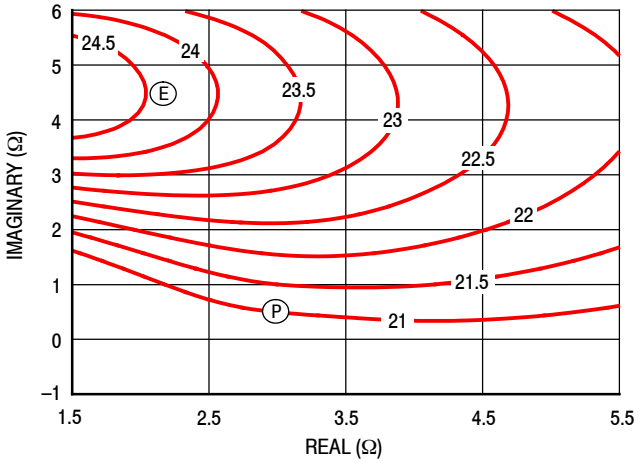


Figure 10. P1dB Load Pull Gain Contours (dB)

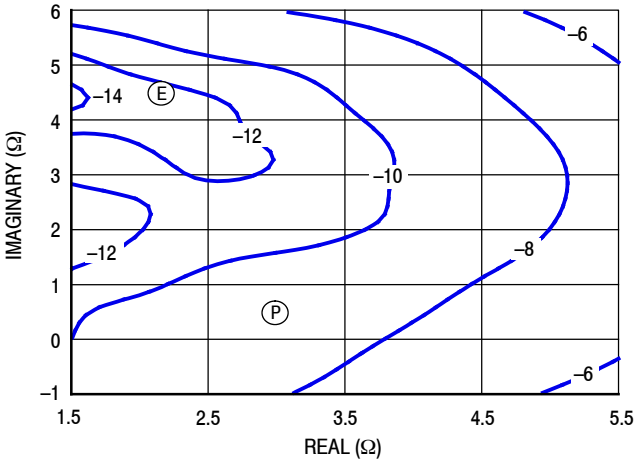


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 652 MHz

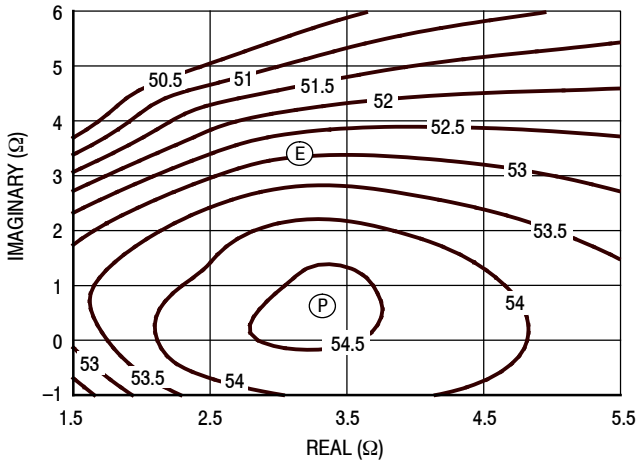


Figure 12. P3dB Load Pull Output Power Contours (dBm)

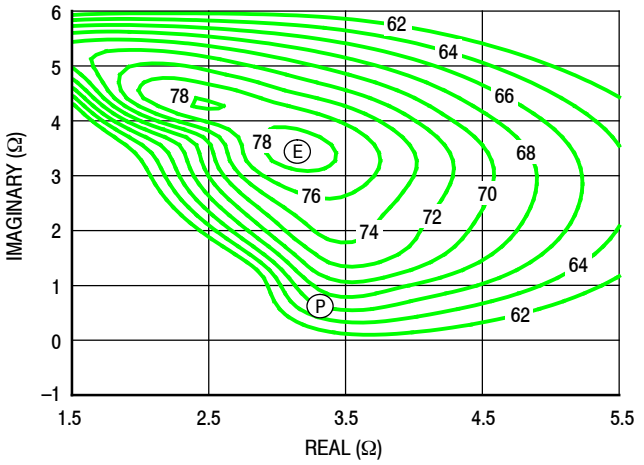


Figure 13. P3dB Load Pull Efficiency Contours (%)

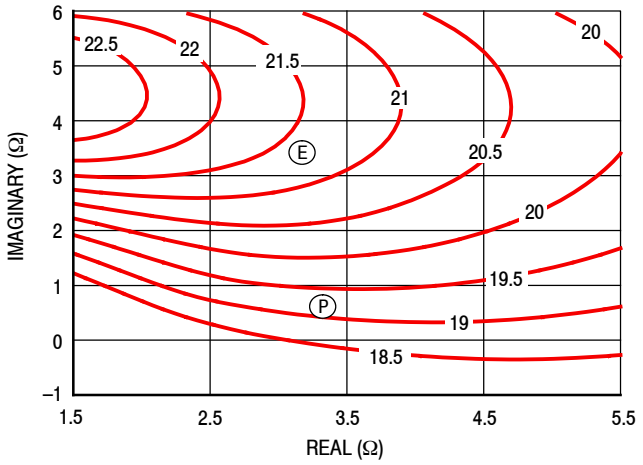


Figure 14. P3dB Load Pull Gain Contours (dB)

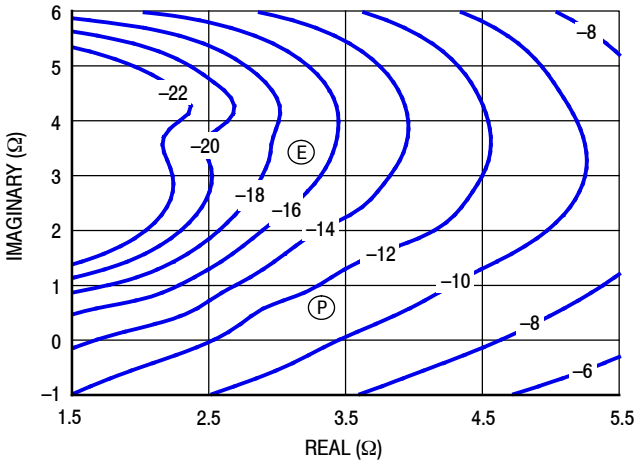


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 652 MHz

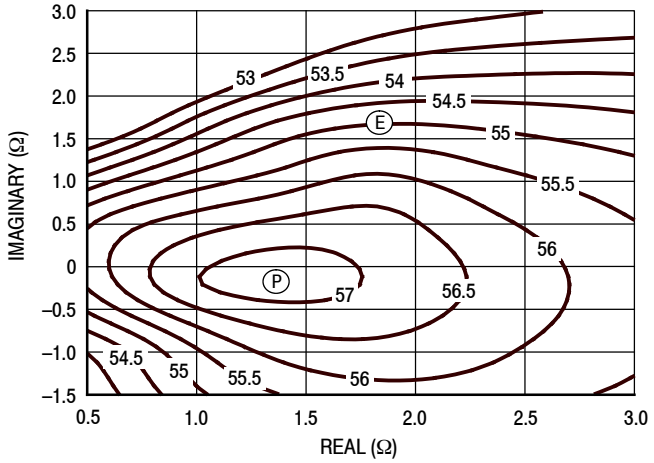


Figure 16. P1dB Load Pull Output Power Contours (dBm)

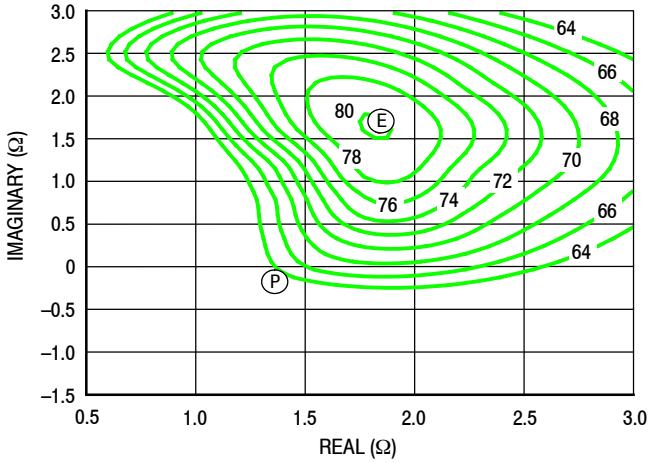


Figure 17. P1dB Load Pull Efficiency Contours (%)

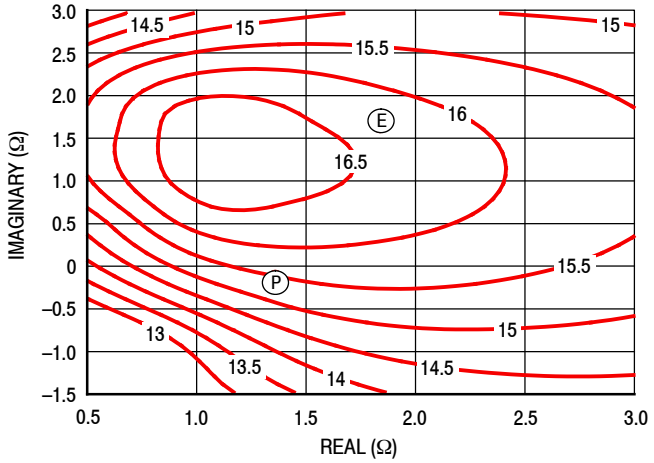


Figure 18. P1dB Load Pull Gain Contours (dB)

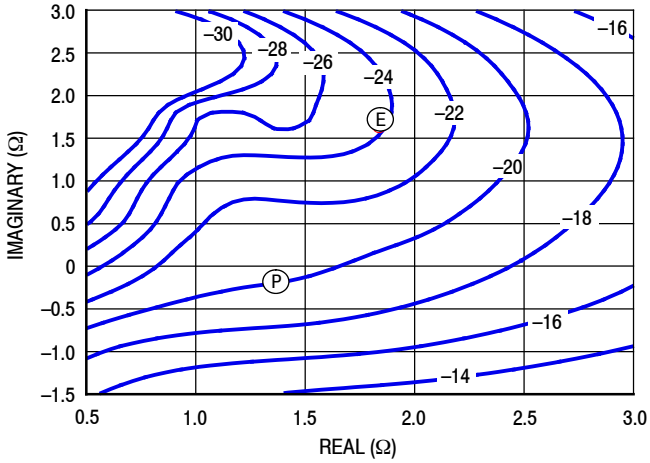


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 652 MHz

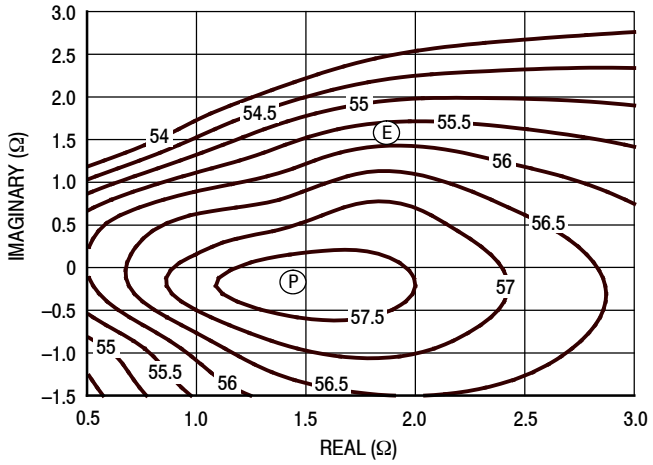


Figure 20. P3dB Load Pull Output Power Contours (dBm)

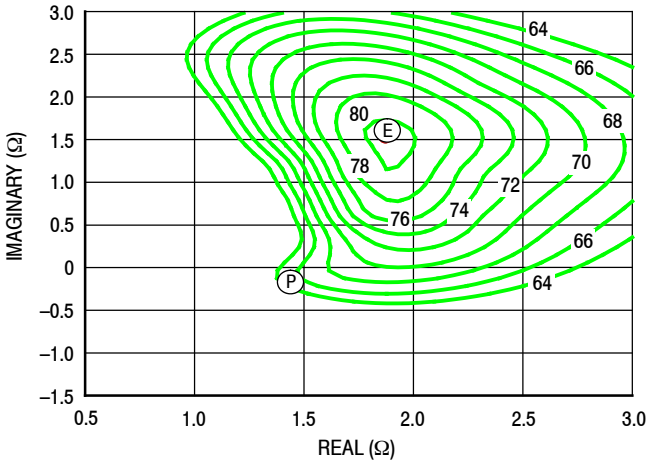


Figure 21. P3dB Load Pull Efficiency Contours (%)

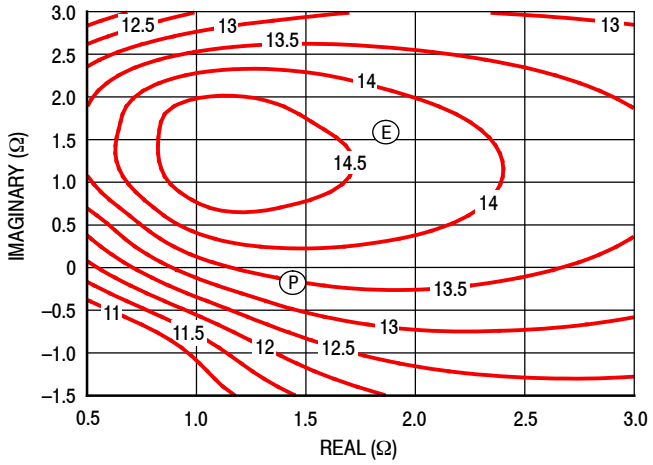


Figure 22. P3dB Load Pull Gain Contours (dB)

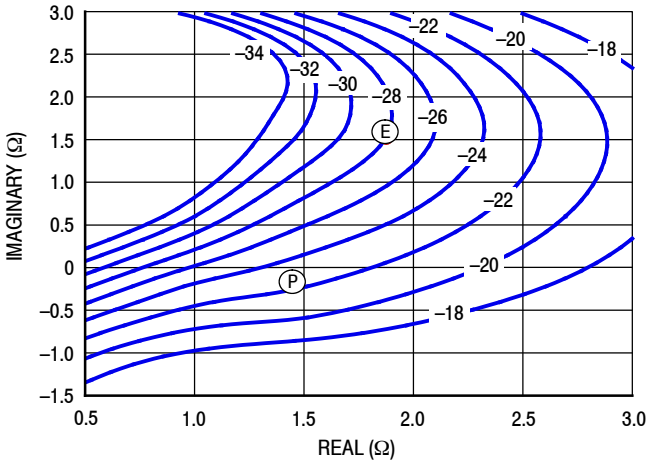


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

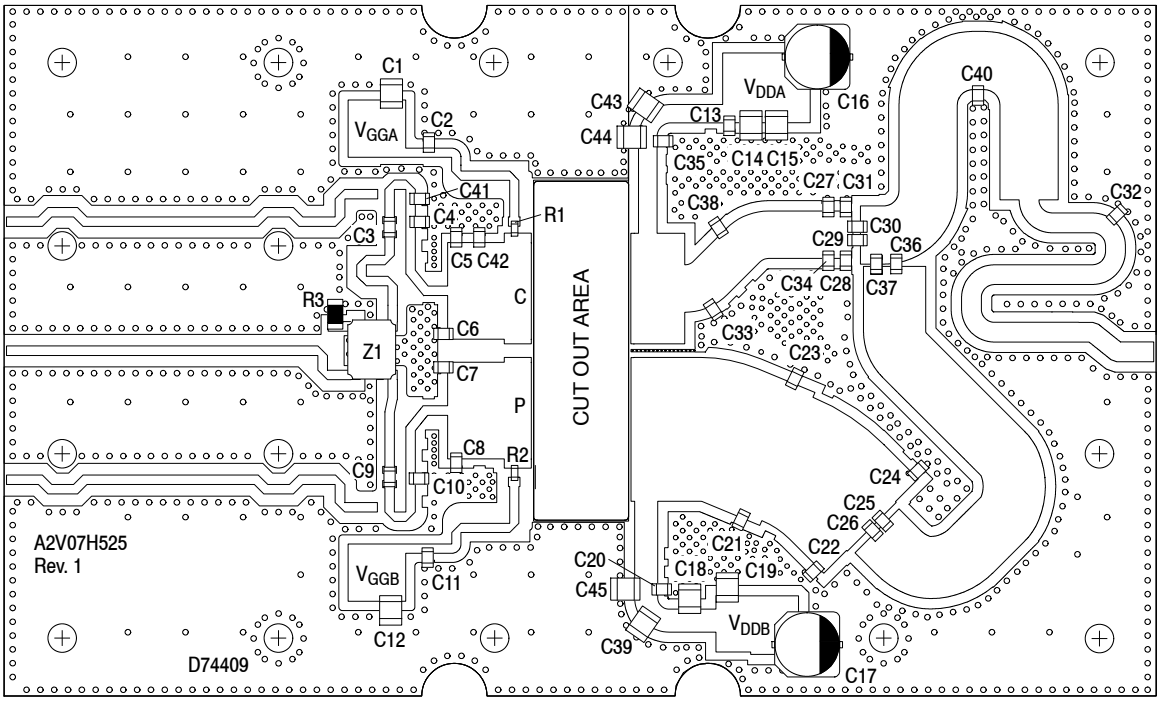


Figure 24. A2V07H525-04NR6 Test Circuit Component Layout — 758–803 MHz

Table 12. A2V07H525-04NR6 Test Circuit Component Designations and Values — 758–803 MHz

Part	Description	Part Number	Manufacturer
C1, C12, C14, C15, C18, C19	10 μF Chip Capacitor	GRM31CR61H106KA12L	Murata
C2, C3, C9, C11, C20, C36, C37	100 pF Chip Capacitor	ATC600F101JT250XT	ATC
C4, C42	1.5 pF Chip Capacitor	ATC600F1R5JT250XT	ATC
C5, C21, C23	8.2 pF Chip Capacitor	ATC600F8R2JT250XT	ATC
C6	1.2 pF Chip Capacitor	ATC600F1R2JT250XT	ATC
C7	3.9 pF Chip Capacitor	ATC600F3R9JT250XT	ATC
C8, C30	12 pF Chip Capacitor	ATC600F120JT250XT	ATC
C10	6.8 pF Chip Capacitor	ATC600F6R8JT250XT	ATC
C13	56 pF Chip Capacitor	ATC600F560JT250XT	ATC
C16, C17	220 μF, 100 V Electrolytic Capacitor	EEV-FK2A221M	Panasonic
C22, C38	5.6 pF Chip Capacitor	ATC600F5R6JT250XT	ATC
C24, C28	5.1 pF Chip Capacitor	ATC600F5R1JT250XT	ATC
C25, C26	39 pF Chip Capacitor	ATC600F390JT250XT	ATC
C27	0.5 pF Chip Capacitor	ATC600F0R5JT250XT	ATC
C29	10 pF Chip Capacitor	ATC600F100JT250XT	ATC
C31, C32, C40	4.7 pF Chip Capacitor	ATC600F4R7JT250XT	ATC
C33, C34	3.3 pF Chip Capacitor	ATC600F3R3JT250XT	ATC
C35	47 pF Chip Capacitor	ATC600F470JT250XT	ATC
C39, C43, C44, C45	4.7 μF Chip Capacitor	C4532X7S2A475M230KB	TDK
C41	1.8 pF Chip Capacitor	ATC600F1R8JT250XT	ATC
R1, R2	2.2 Ω, 1/4 W Chip Resistor	CRCW08052R20JNEA	Vishay
R3	50 Ω, 10 W Termination Chip Resistor	C8A50Z4	Anaren
Z1	600–900 MHz, 90°, 3 dB Hybrid Coupler	X3C07P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D74409	MTL

TYPICAL CHARACTERISTICS — 758–803 MHz

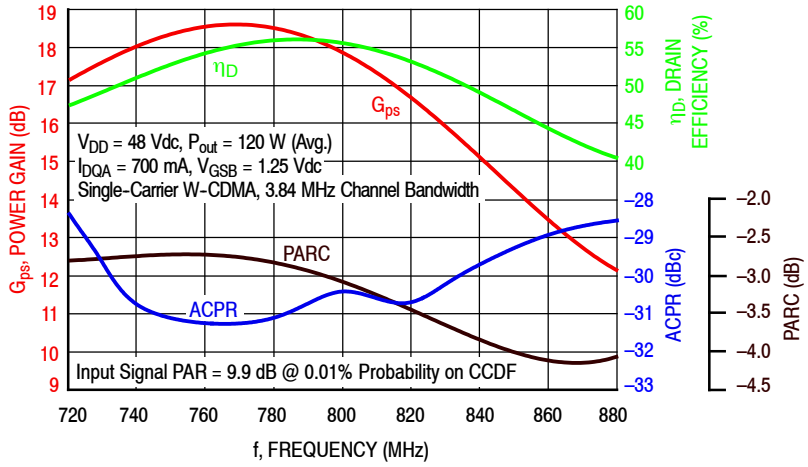


Figure 25. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 120 Watts Avg.

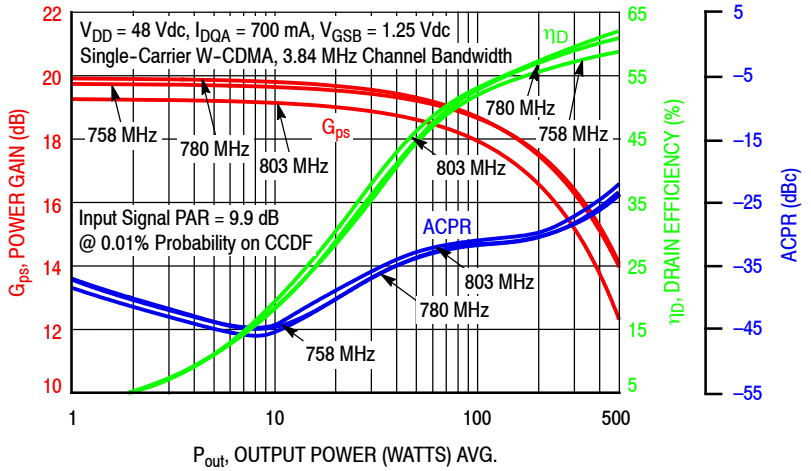


Figure 26. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

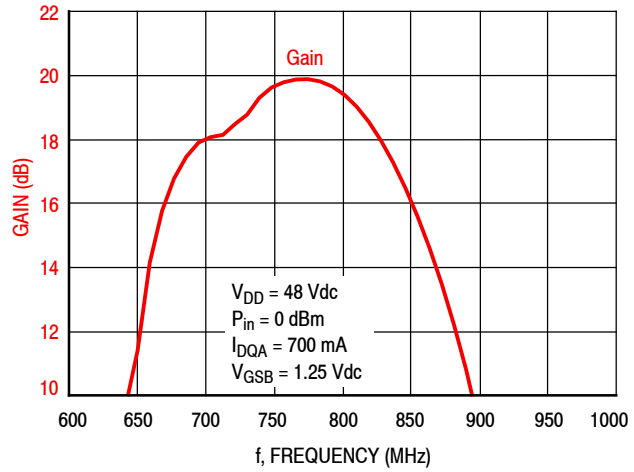


Figure 27. Broadband Frequency Response

Table 13. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 704 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	4.45 – j6.09	4.50 + j6.10	3.66 – j0.70	19.4	53.3	216	51.5	–9
780	4.79 – j7.15	4.67 + j6.96	1.87 + j0.82	20.1	53.5	226	57.5	–5
822	7.09 – j9.84	6.84 + j9.59	1.95 + j0.64	19.6	53.8	241	61.1	–6

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	4.45 – j6.09	4.19 + j6.43	3.55 – j0.55	17.5	54.4	272	56.2	–10
780	4.79 – j7.15	4.57 + j7.46	2.15 + j0.60	18.0	54.6	288	61.5	–9
822	7.09 – j9.84	6.79 + j10.2	2.09 + j0.43	17.4	54.7	292	62.6	–10

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 14. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 704 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	4.45 – j6.09	4.02 + j6.30	3.33 + j2.99	22.1	51.3	133	60.9	–8
780	4.79 – j7.15	4.15 + j7.31	1.98 + j2.84	22.7	51.5	141	71.3	–8
822	7.09 – j9.84	6.11 + j9.97	1.58 + j2.62	22.2	51.1	128	72.3	–12

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	4.45 – j6.09	3.94 + j6.62	3.66 + j2.45	19.7	53.0	198	64.5	–9
780	4.79 – j7.15	4.29 + j7.83	2.49 + j2.82	20.4	52.7	186	72.6	–14
822	7.09 – j9.84	6.31 + j10.7	1.84 + j2.66	20.0	52.0	158	73.6	–19

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

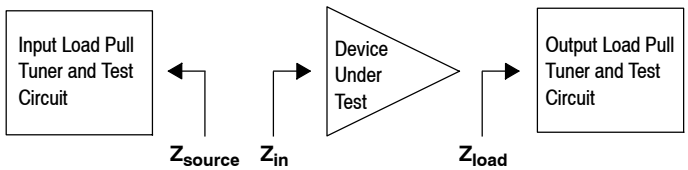


Table 15. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	2.10 – j3.04	2.19 + j3.13	1.06 – j0.27	15.9	57.2	527	60.3	–13
780	2.40 – j3.25	2.40 + j3.54	0.95 – j0.27	15.9	57.4	544	61.9	–11
822	3.26 – j3.95	3.09 + j4.47	0.89 – j0.43	15.4	57.2	520	60.4	–10

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	2.10 – j3.04	1.99 + j3.42	1.08 – j0.31	13.8	58.1	641	63.9	–19
780	2.40 – j3.25	2.19 + j3.88	1.00 – j0.32	13.8	58.1	650	65.0	–17
822	3.26 – j3.95	2.91 + j4.94	1.01 – j0.55	13.4	57.9	620	62.8	–15

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

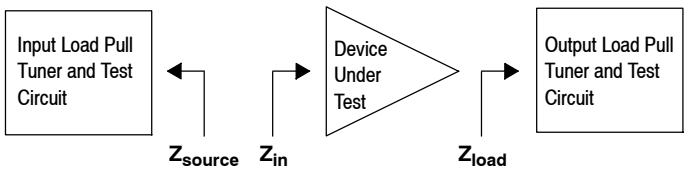
Table 16. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 1.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	2.10 – j3.04	1.61 + j2.90	1.11 + j1.20	18.1	54.3	269	75.7	–18
780	2.40 – j3.25	1.86 + j3.36	1.18 + j0.85	18.0	55.1	320	75.8	–15
822	3.26 – j3.95	2.42 + j4.28	0.99 + j0.53	17.4	55.0	316	74.7	–16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	2.10 – j3.04	1.67 + j3.33	1.49 + j0.80	15.8	56.3	426	74.8	–22
780	2.40 – j3.25	1.82 + j3.79	1.41 + j0.69	15.8	56.2	419	74.3	–22
822	3.26 – j3.95	2.35 + j4.75	1.06 + j0.54	15.5	55.6	366	74.3	–24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 780 MHz

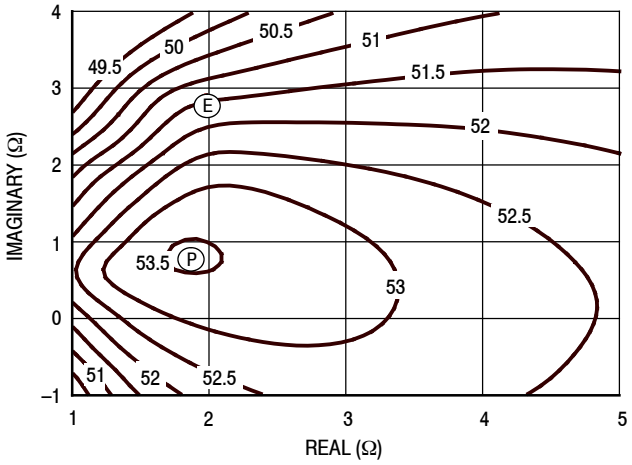


Figure 28. P1dB Load Pull Output Power Contours (dBm)

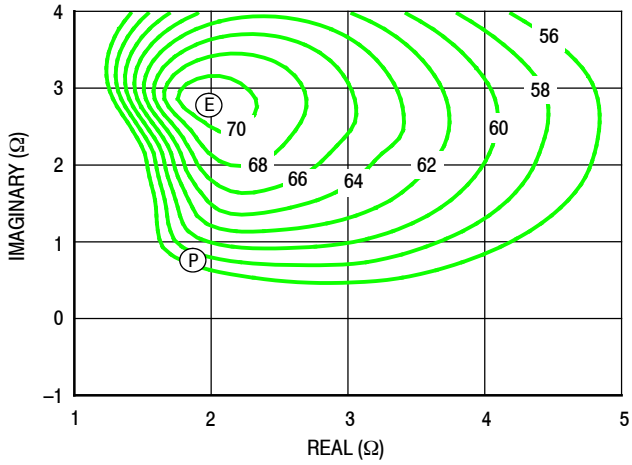


Figure 29. P1dB Load Pull Efficiency Contours (%)

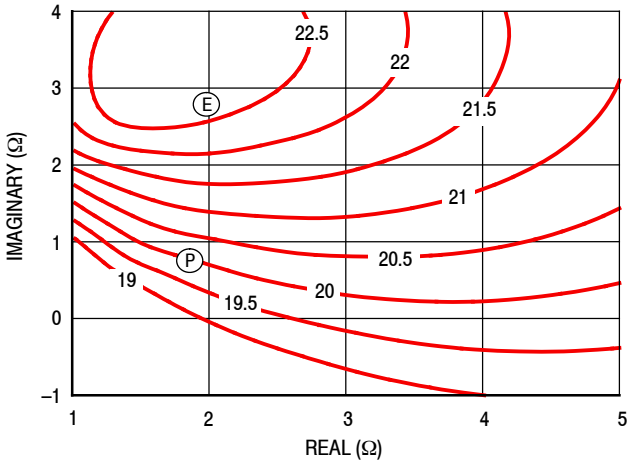


Figure 30. P1dB Load Pull Gain Contours (dB)

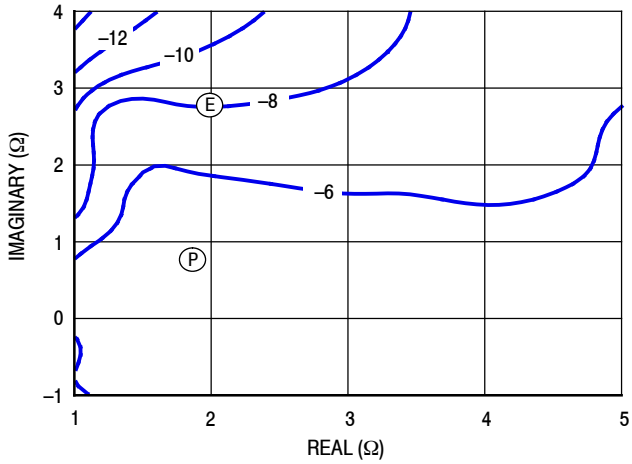


Figure 31. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 780 MHz

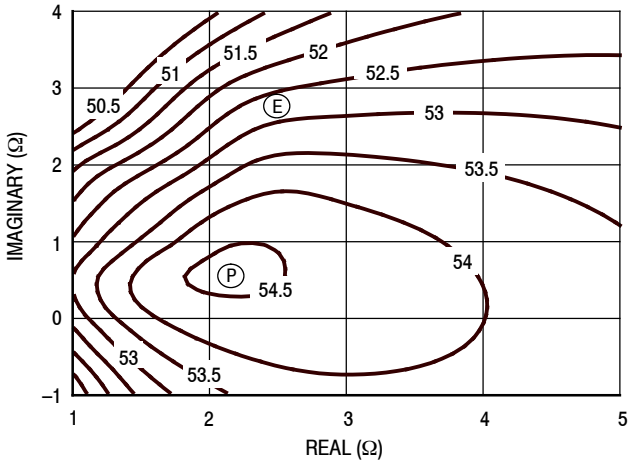


Figure 32. P3dB Load Pull Output Power Contours (dBm)

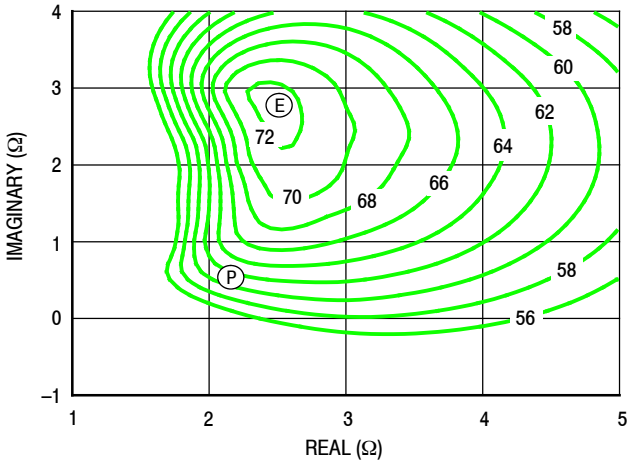


Figure 33. P3dB Load Pull Efficiency Contours (%)

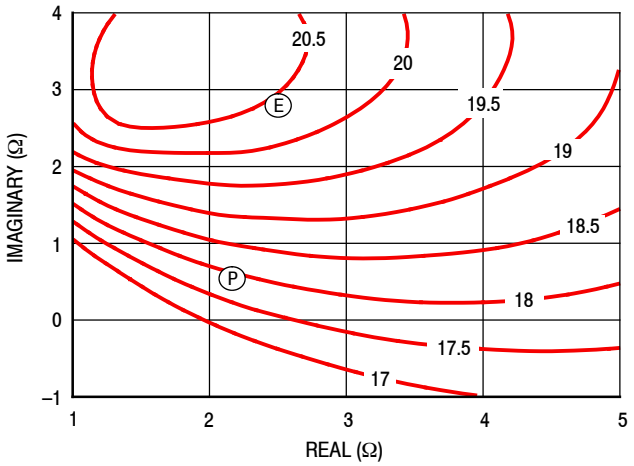


Figure 34. P3dB Load Pull Gain Contours (dB)

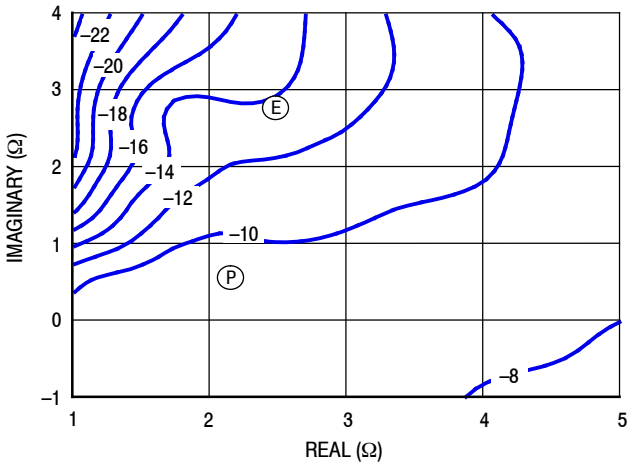


Figure 35. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 780 MHz

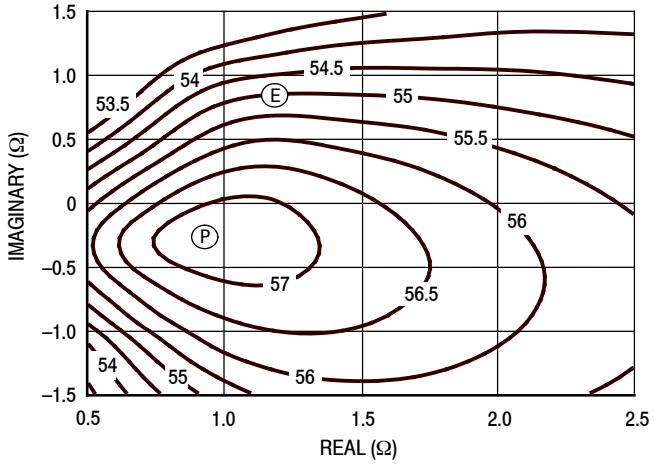


Figure 36. P1dB Load Pull Output Power Contours (dBm)

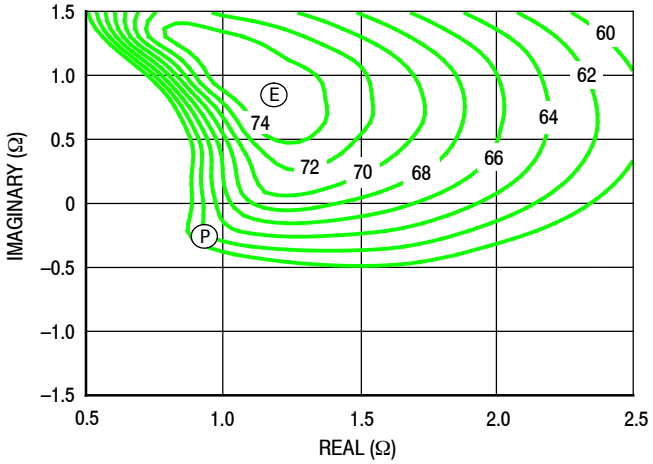


Figure 37. P1dB Load Pull Efficiency Contours (%)

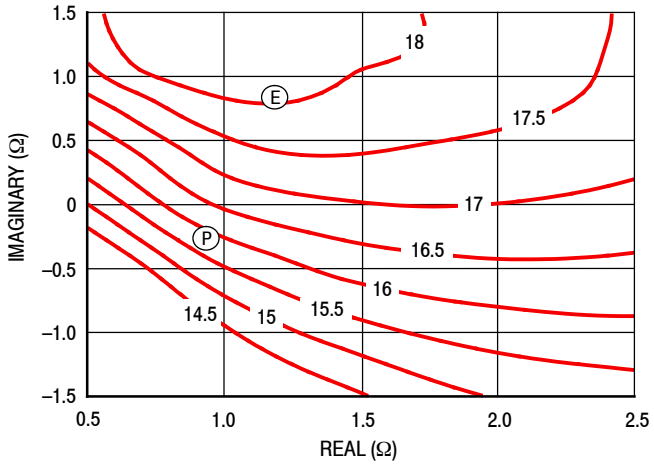


Figure 38. P1dB Load Pull Gain Contours (dB)

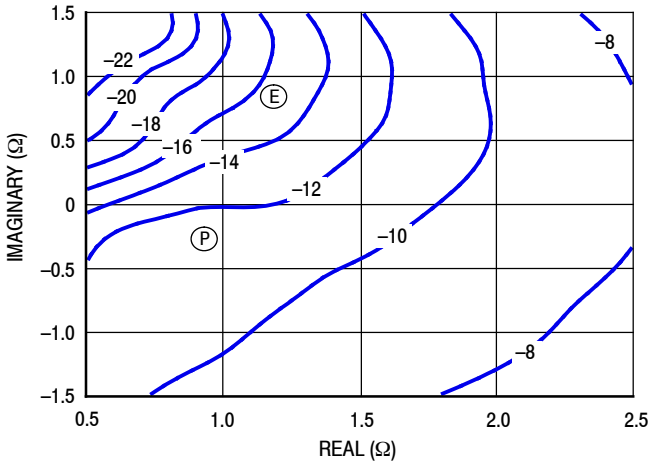


Figure 39. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 780 MHz

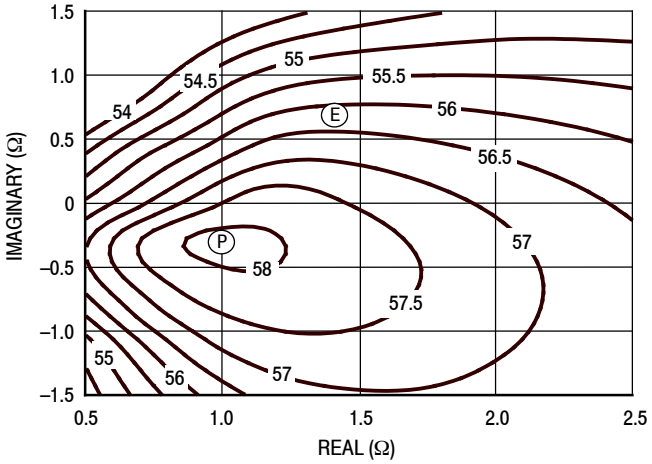


Figure 40. P3dB Load Pull Output Power Contours (dBm)

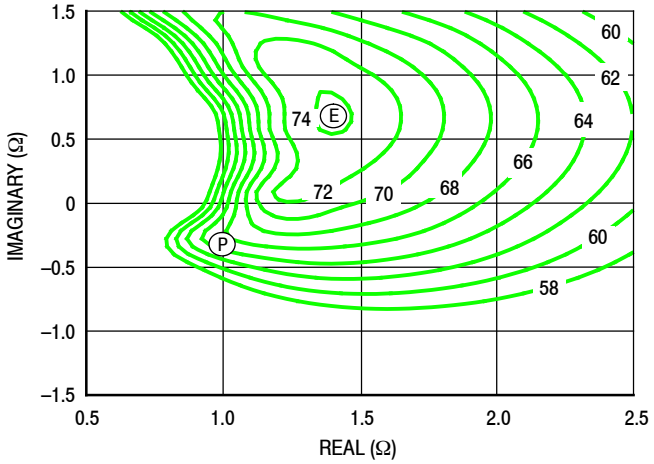


Figure 41. P3dB Load Pull Efficiency Contours (%)

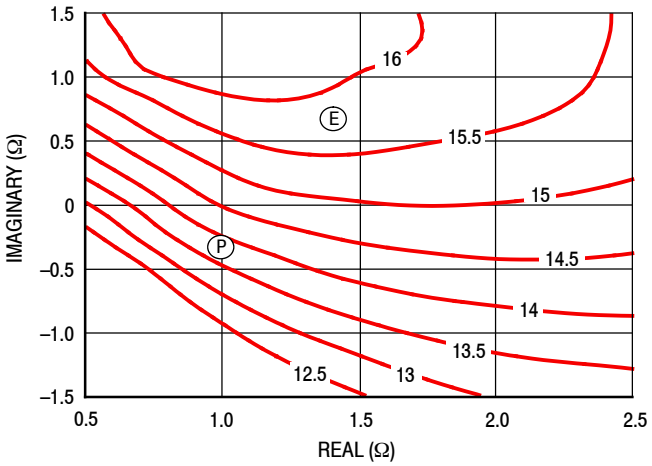


Figure 42. P3dB Load Pull Gain Contours (dB)

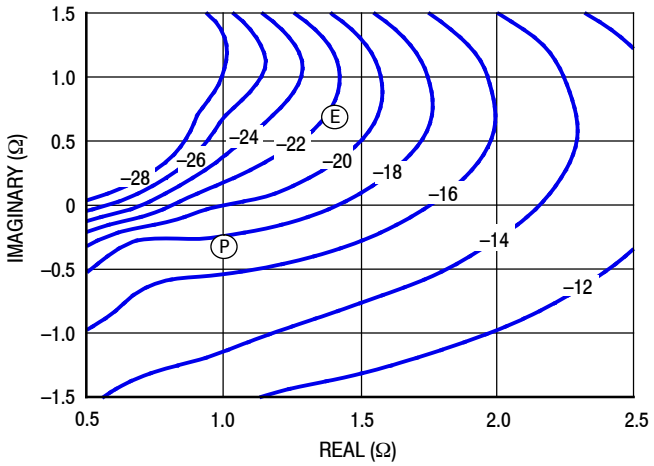


Figure 43. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

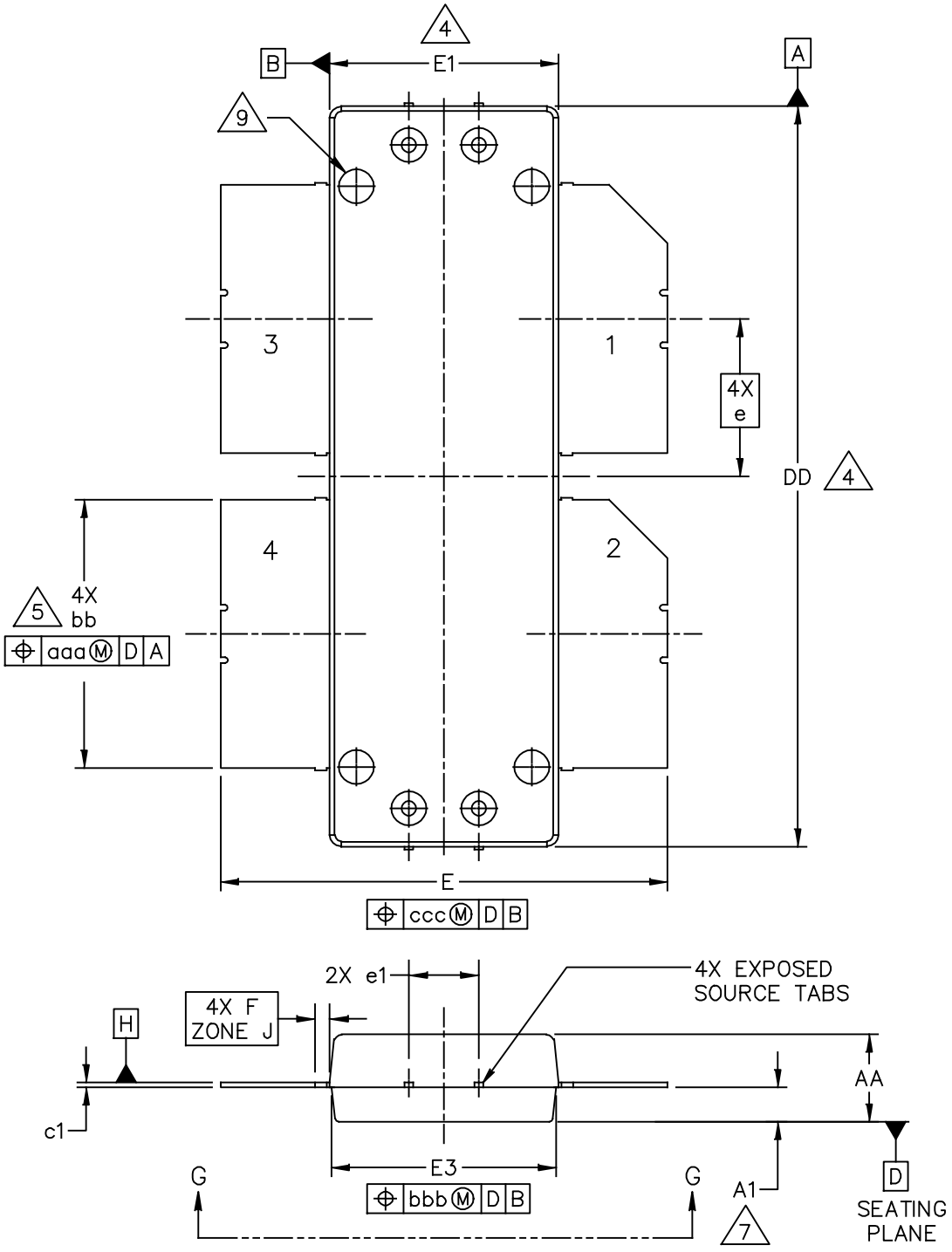
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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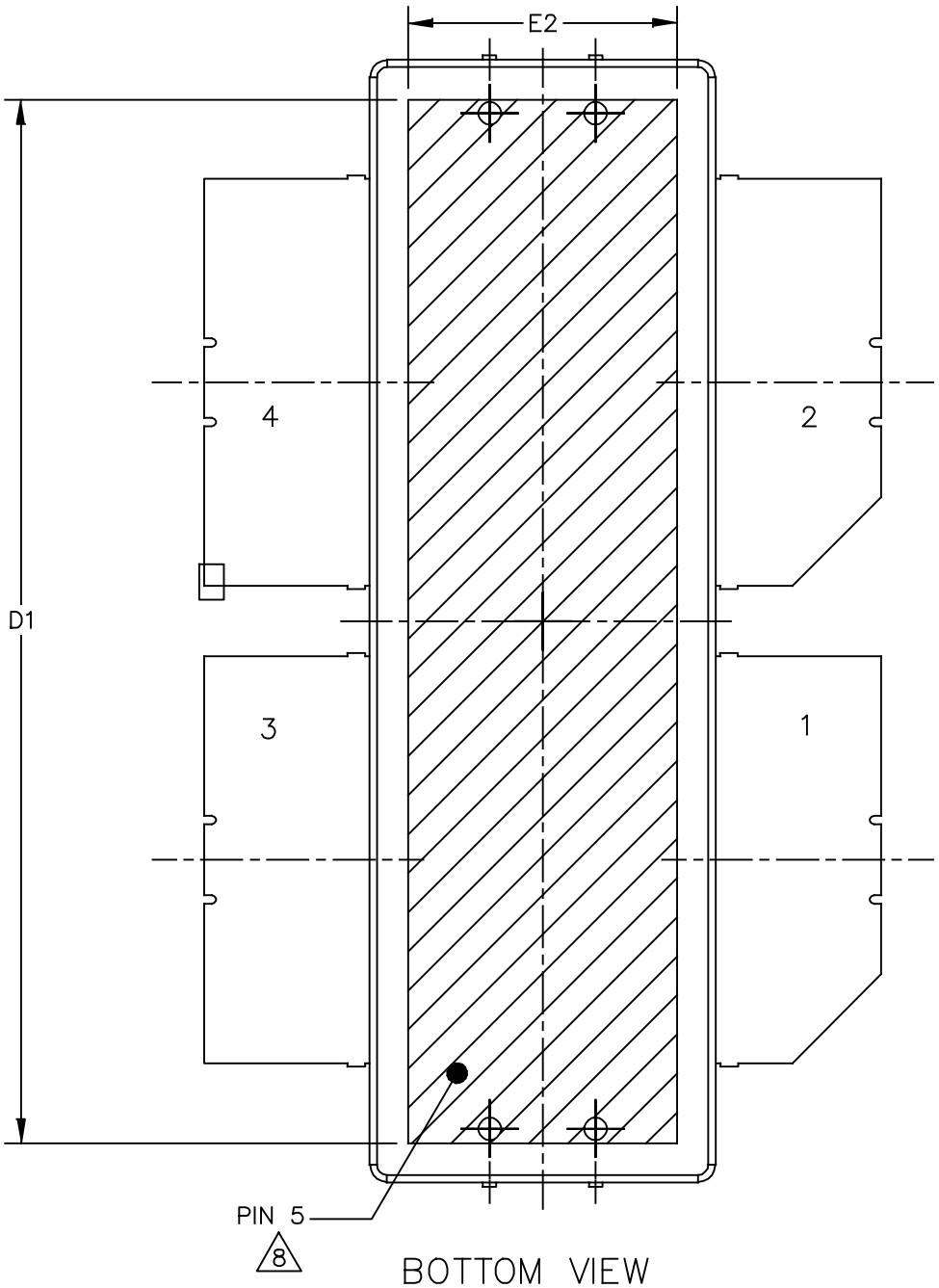
	STANDARD: NON-JEDEC	
	SOT1816-1	08 FEB 2016



BOTTOM VIEW
VIEW G–G

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	STANDARD: NON–JEDEC	
	SOT1816–1	08 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A1 APPLIES WITHIN ZONE J ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	bb	.457	.463	11.61	11.76
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
DD	1.267	1.273	32.18	32.33	e	.270 BSC		6.86 BSC	
D1	1.180	----	29.97	----	e1	.116	.124	2.95	3.15
E	.762	.770	19.35	19.56					
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----	bbb	.006		0.15	
E3	.383	.387	9.73	9.83	ccc	.010		0.25	
F	.025 BSC		0.635 BSC						

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: OM–1230–4L

DOCUMENT NO: 98ASA00506D REV: C

STANDARD: NON–JEDEC

SOT1816–1 08 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2017	• Initial release of data sheet

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Document Number: A2V07H525-04N
Rev. 0, 07/2017