REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add the statements to paragraphs 3.1 and 3.5.1 to allow manufacturer to meet the die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535. Update boilerplate. Editorial changes throughout.	00-03-30	Monica L. Poelking
B	Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-08-22	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Ray Monnin

CHECKED BY
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APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
87-05-01

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, UNIVERSAL INTERRUPT CONTROLLER, N-CHANNEL MOS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87597**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E414-05

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87597	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	9519A	Universal interrupt controller

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7 V dc
Input voltage range	-0.5 V dc to +7 V dc
Maximum power dissipation (P_D)	1.5 W 1/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum low level input voltage (V_{IL})	-0.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Maximum high level input voltage (V_{IH})	V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 of other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Switching waveforms. The switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		All	1, 2, 3		0.8	V
Input high voltage	V_{IH}		All	1, 2, 3	2.0		V
Output low voltage	V_{OL1}	V_{CC} = 4.5 V, I_{OL} = 3.2 mA	All	1, 2, 3		0.40	V
Output low voltage (EO only)	V_{OL2}	V_{CC} = 4.5 V, I_{OL} = 1.0 mA	All	1, 2, 3		0.40	V
Output high voltage 1/	V_{OH1}	V_{CC} = 4.5 V, I_{OH} = -200 µA	All	1, 2, 3	2.4		V
Output high voltage (EO only)	V_{OH2}	V_{CC} = 4.5 V, I_{OH} = -100 µA	All	1, 2, 3	2.4		V
Output float leakage	I_{OZ}	V_{CC} = 5.5 V V_{OUT} = 5.5 V and 0.0 V Output off	All	1, 2, 3	-150	+150	µA
Input leakage	I_{IX1}	V_{CC} = 5.5 V V_{IN} = 5.5 V and 0.0 V	All	1, 2, 3	-10	+10	µA
Input leakage (EI only)	I_{IX2}	V_{CC} = 5.5 V V_{IN} = 5.5 V and 0.0 V	All	1, 2, 3	-60	+10	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V 2/	All	1, 2, 3		200	mA
Input capacitance	C_{IN}	T_A = +25°C f_C = 1 MHz See 4.3.1d	All	4		10	pF
Outptut capacitance	C_{OUT}			4		15	
I/O capacitance	$C_{I/O}$			4		20	
Functional test		See 4.3.1c	All	7, 8			
C/$\overline{D}$ valid and $\overline{CS}$ low to READ low	t_{AVRL}	3/ 4/	All	9, 10, 11	0		ns
C/$\overline{D}$ valid and $\overline{CS}$ low to WRITE low	t_{AVWL}		All	9, 10, 11	0		ns
$\overline{RIP}$ low to $\overline{PAUSE}$ high 5/	t_{CLPH}		All	9, 10, 11	75	375	ns
$\overline{RIP}$ low to data out valid 6/	t_{CLQV}		All	9, 10, 11		50	ns
Data in valid to write high	t_{DVWH}		All	9, 10, 11	250		ns
EI high to $\overline{RIP}$ low 7/	t_{EHCL}		All	9, 10, 11	30	300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Interrupt request valid to GINT valid	t_{IVGV}	3/ 4/	All	9, 10, 11	100	800	ns
Interrupt request valid to interrupt request don't care. (IREQ pulse duration)	t_{IVIX}		All	9, 10, 11	250		ns
$\overline{IACK}$ high to $\overline{RIP}$ high	t_{KHCH}		All	9, 10, 11		450	ns
$\overline{IACK}$ high to GINT invalid	t_{KHIH}		All	9, 10, 11		1000	ns
$\overline{IACK}$ high to $\overline{IACK}$ low ($\overline{IACK}$ recovery)	t_{KHKL}		All	9, 10, 11	140		ns
$\overline{IACK}$ high to EO high 8/ 9/	t_{KHNH}		All	9, 10, 11		975	ns
$\overline{IACK}$ high to data out invalid	t_{KHQX}		All	9, 10, 11	20	200	ns
$\overline{IACK}$ low to $\overline{RIP}$ low 7/ 10/	t_{KLCL}		All	9, 10, 11	75	650	ns
$\overline{IACK}$ low to $\overline{IACK}$ high (1^{st} $\overline{IACK}$) 10/	t_{KLKH}		All	9, 10, 11	975		ns
$\overline{IACK}$ low to EO low 8/ 9/ 10/	t_{KLNL}		All	9, 10, 11		125	ns
$\overline{IACK}$ low to $\overline{PAUSE}$ low 10/	t_{KLPL}		All	9, 10, 11	25	175	ns
$\overline{IACK}$ low to data out valid 6/ 10/	t_{KLQV}		All	9, 10, 11	25	300	ns
1^{st} $\overline{IACK}$ low to data out valid 10/	t_{KLQV1}		All	9, 10, 11	75	650	ns
$\overline{PAUSE}$ high to $\overline{IACK}$ low	t_{PHKH}		All	9, 10, 11	0		ns
Read high to C/$\overline{D}$ and $\overline{CS}$ don't care	t_{RHAX}		All	9, 10, 11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Read low to data out valid	t_{RLQV}	3/ 4/	All	9, 10, 11		300	ns
Read high to data out invalid	t_{RHQX}		All	9, 10, 11	20	200	ns
Read low to data out unknown	t_{RLQX}		All	9, 10, 11	35		ns
Read low to read high ($\overline{RD}$ pulse duration)	t_{RLRH}		All	9, 10, 11	300		ns
Write high to C/$\overline{D}$ and $\overline{CS}$ don't care	t_{WHAX}		All	9, 10, 11	25		ns
Write high to data in don't care	t_{WHDX}		All	9, 10, 11	25		ns
Write high to read or write low ($\overline{WR}$ recovery)	t_{WHRW}		All	9, 10, 11	600		ns
Write low to write high ($\overline{WR}$ pulse duration)	t_{WLWH}		All	9, 10, 11	300		ns

1/ V_{OH} specifications do not apply to $\overline{RIP}$, $\overline{PAUSE}$, or GINT when active low. These outputs are open-drain and V_{OH} levels will be determined by external circuitry.

2/ I_{CC} is measured in a static condition with outputs in the worst condition with all outputs unloaded.

3/ Test conditions:
V_{IL} = 0.45 V, V_{IH} = 2.4 V
V_{OL} = 0.8 V, V_{OH} = 2.0 V
I_{OL} = 3.2 mA, I_{OH} = -200 µA
I_{OL} = 1.0 mA, I_{OH} = -100 µA (EO only)
C_L = 100 pF

4/ See figure 4.

5/ During the first $\overline{IACK}$ pulse, $\overline{PAUSE}$ will be low long enough to allow for priority resolution and will not go high until after $\overline{RIP}$ goes low (t_{CLPH}).

6/ t_{KLQV} applies only to second, third, and fourth $\overline{IACK}$ pulses while $\overline{RIP}$ is low. During the first $\overline{IACK}$ pulse, data out will be valid following the falling edge of $\overline{RIP}$ (t_{CLQV}).

7/ $\overline{RIP}$ is pulled low to indicate that an interrupt request has been selected. $\overline{RIP}$ cannot be pulled low until EI is high following an internal delay. t_{KLCL} will govern the falling edge of $\overline{RIP}$ when EI is always high or is high early in the acknowledge cycle. t_{EHCL} will gevern when EI goes high later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. $\overline{RIP}$ remains low until after the rising edge of $\overline{IACK}$ pulse that transfers the last response byte for selected IREQ.

8/ Test conditions for EO assume an output loading of I_{OL} = 1.0 mA and I_{OH} = -100 µA.

9/ The arrival of $\overline{IACK}$ will cause EO to go low, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return high when EI is high. If a pending request is selected, EO will stay low until after the last $\overline{IACK}$ pulse for that interrupt is complete and $\overline{RIP}$ goes high.

10/ $\overline{CS}$ must be high for at least 100 ns prior to $\overline{IACK}$ going low.

Device type	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{CS}$	15	$\overline{PAUSE}$
2	$\overline{WR}$	16	EO
3	$\overline{RD}$	17	GINT
4	DB_7	18	$IREQ_0$
5	DB_6	19	$IREQ_1$
6	DB_5	20	$IREQ_2$
7	DB_4	21	$IREQ_3$
8	DB_3	22	$IREQ_4$
9	DB_2	23	$IREQ_5$
10	DB_1	24	$IREQ_6$
11	DB_0	25	$IREQ_7$
12	$\overline{RIP}$	26	$\overline{IACK}$
13	EI	27	$C/\overline{D}$
14	V_{SS} (GND)	28	V_{CC} (+5 V)

FIGURE 1. Terminal connections.

Device type	All		
Case outline	Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	23	NC
2	$\overline{CS}$	24	$\overline{PAUSE}$
3	$\overline{WR}$	25	EO
4	$\overline{RD}$	26	GINT
5	NC	27	NC
6	NC	28	NC
7	NC	29	NC
8	NC	30	$IREQ_0$
9	DB_7	31	$IREQ_1$
10	DB_6	32	$IREQ_2$
11	DB_5	33	$IREQ_3$
12	DB_4	34	$IREQ_4$
13	DB_3	35	$IREQ_5$
14	DB_2	36	$IREQ_6$
15	DB_1	37	$IREQ_7$
16	DB_0	38	NC
17	NC	39	NC
18	NC	40	NC
19	$\overline{RIP}$	41	$\overline{IACK}$
20	EI	42	$C/\overline{D}$
21	V_{SS} (GND)	43	V_{CC} (+5 V)
22	NC	44	NC

NC = No connection

FIGURE 1. Terminal connections - Continued.

Control Input					Data bus operation
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{IACK}$	
0	0	0	1	1	Transfer contents of preselected data register to data bus
0	0	1	0	1	Transfer contents of data bus to preselected data register
0	1	1	0	1	Transfer contents of status register to data bus
0	1	1	0	1	Transfer contents of data bus to command register
1	X	X	X	0	Transfer contents of selected response memory location to data bus
1	X	X	X	1	No information transferred

Command code								Command description
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear all IRR and IMR bits specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR
0	0	1	0	1	B2	B1	B0	Clear IMR bits specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bits specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bits specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bits specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bits specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load mode register bits 0-4 with specified pattern
1	0	1	0	M6	M5	0	0	Load mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselected IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselected auto clear register for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

FIGURE 2. Truth tables.

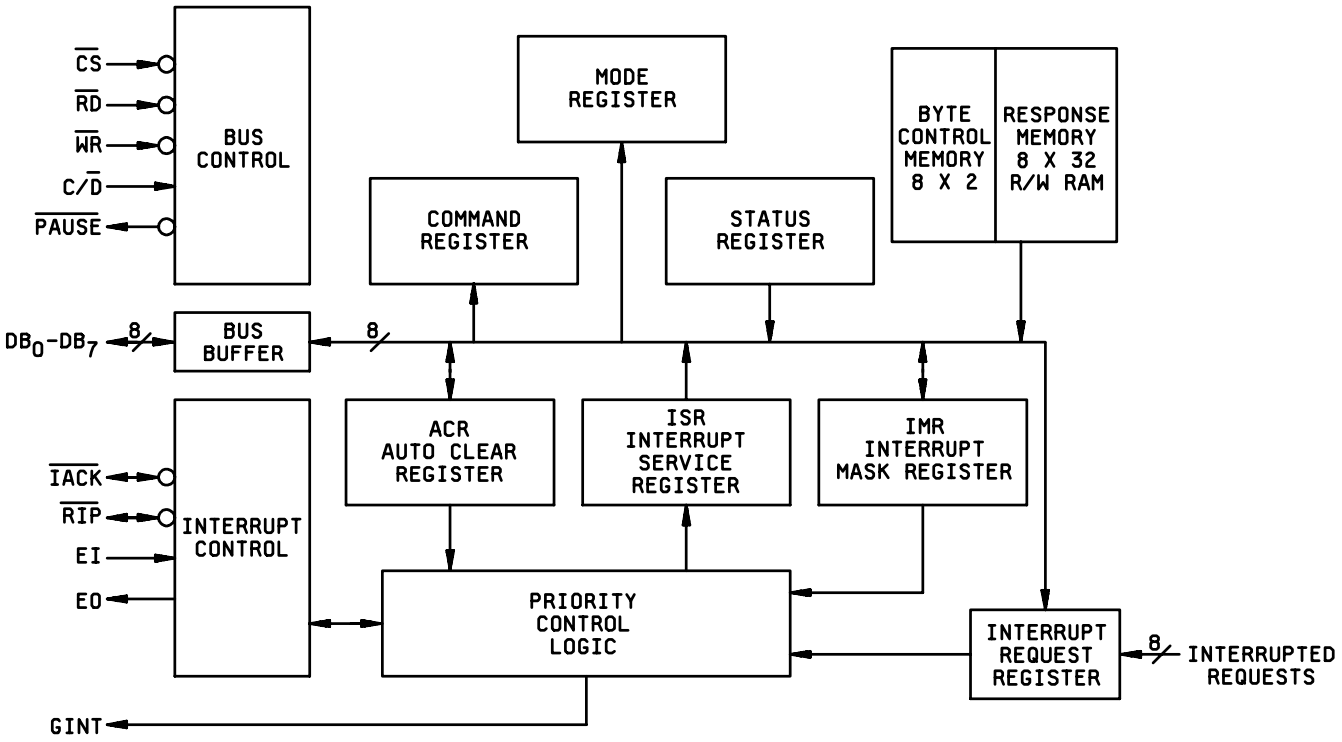
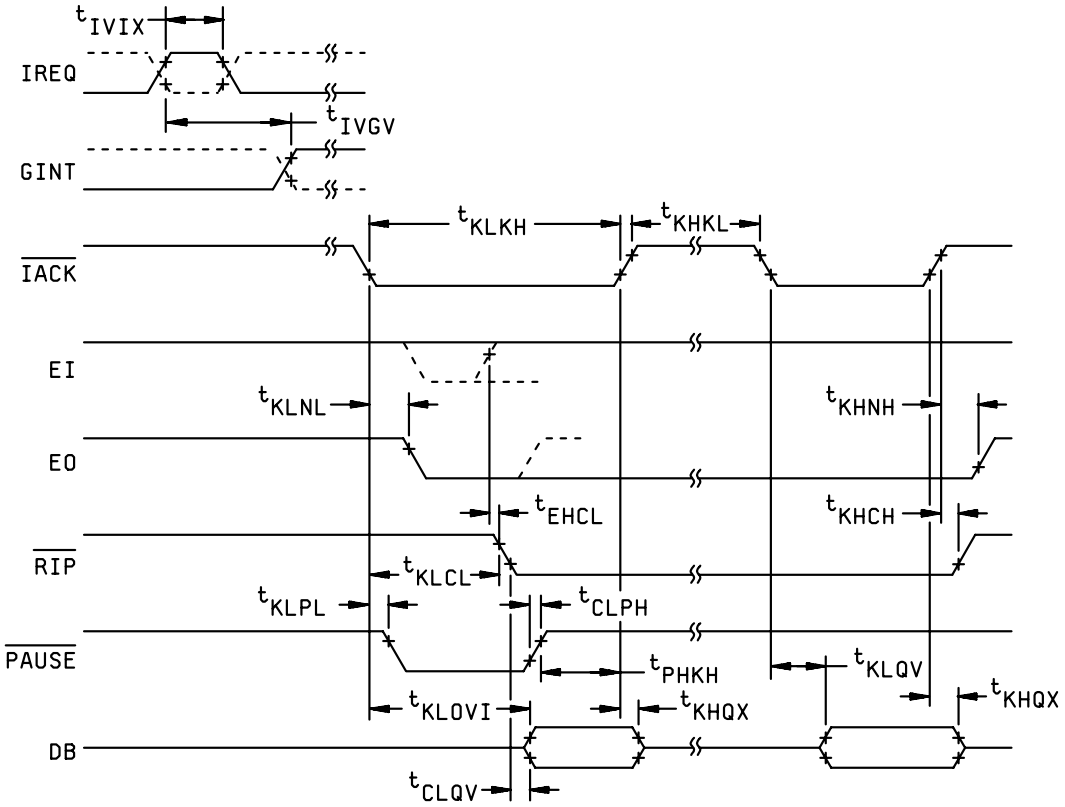
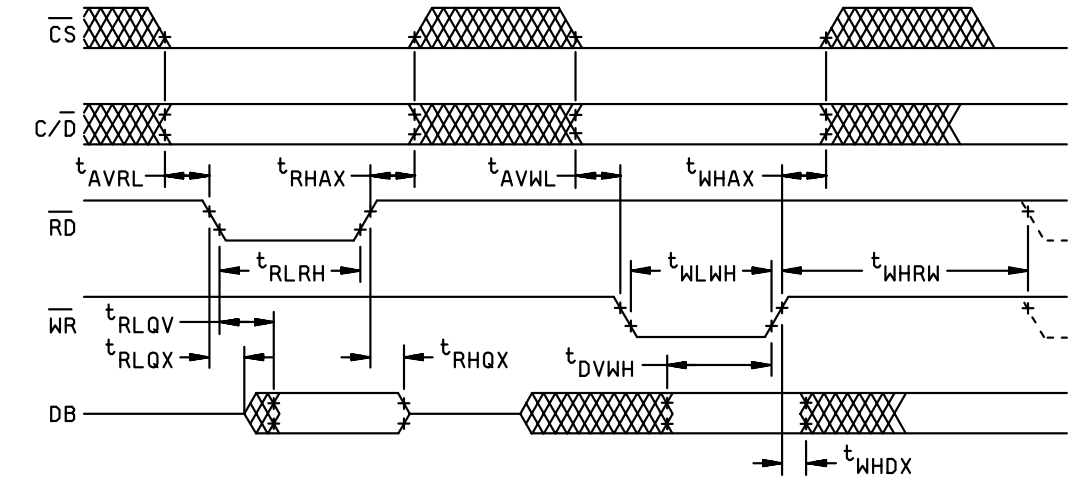


FIGURE 3. Block diagram.



INTERRUPT OPERATIONS



DATA BUS TRANSFERS

FIGURE 4. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth tables.

d. Subgroup 4 (C_{IN}, C_O, $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-08-22

Approved sources of supply for SMD 5962-87597 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8759701XA	0C7V7	9519A/XA
5962-8759701XA	3V146	9519A/BXA
5962-8759701YA	0C7V7	9519A/YA
5962-8759701YA	3V146	9519A/BYA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
3V146	Rochester electronics 10 Malcolm Hoyt Drive Newburyport, MA 01950

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