REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Delete programming waveforms, 4.5.1, 4.5.2, and table III. Changes to 4.5 and 6.6. Editorial changes throughout. Redrawn.	90-06-25	M. Poelking
D	Change C_{IN} and C_{OUT} in table I, IAW NOR 5962-R003-9l.	91-09-20	M. A. Frye
E	Add device type 05; editorial changes throughout. Redrawn.	93-02-02	M. A. Frye
F	Add device type 06; editorial changes throughout. Redrawn.	93-05-04	M. A. Frye
G	Changes in accordance with NOR 5962-R187-93	93-06-17	M. A. Frye
H	Changes in accordance with NOR 5962-R207-93	93-07-29	M. A. Frye
J	Update drawing to current requirements. Editorial changes throughout. - gap	02-01-04	Raymond Monnin
K	Boilerplate update, part of 5 year review. ksr	08-04-25	Robert M. Heber
L	Corrected I_{IL} and I_{IH} parameters in Table I. ksr	10-03-29	Charles F. Saffle

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	L																			
SHEET	15																			

REV STATUS	REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
M. A. Frye

DRAWING APPROVAL DATE
87-10-20

REVISION LEVEL
L

MICROCIRCUIT, MEMORY, DIGITAL, CMOS UV ERASABLE, PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87539**

SHEET 1 OF 15

DSCC FORM 2233
APR 97

5962-E254-10

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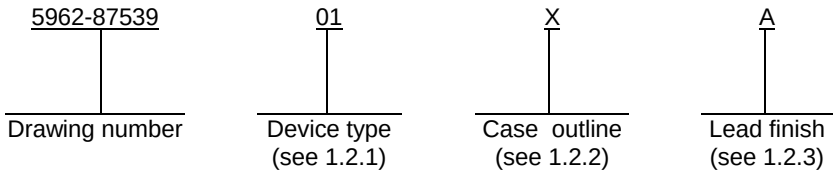
1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}
01	C22V10	22-input 10-output AND-OR-logic array	25 ns
02	C22V10	22-input 10-output AND-OR-logic array	30 ns
03	C22V10	22-input 10-output AND-OR-logic array	40 ns
04	C22V10	22-input 10-output AND-OR-logic array	20 ns
05	C22V10	22-input 10-output AND-OR-logic array	15 ns
06	C22V10	22-input 10-output AND-OR-logic array	10 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24, CDFP3-F24	24	Flat package 1/
L	GDIP3-T24, CDIP4-T24	24	Dual-in-line package 1/
3	CQCC1-N28	28	Square chip carrier package 1/
X	GQCC1-J28	28	"J" lead chip carrier package 1/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 3/
Output voltage applied range	-0.5 V dc to +7.0 V dc 3/
Output sink current	16 mA
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D) 4/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.
3/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. Defense Supply Center Columbus (DSCC), DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.11 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.11.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.11.3 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.5 herein) to the specified pattern or erased (see 4.4 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{SS} = 0 V -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -2.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 12.0 mA	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_O = GND and V_O = 5.5 V V_{CC} = 5.5 V	1, 2, 3	All	-40	40	µA
High level input current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All	-10	+10	µA
Low level input current	I_{IL}	V_{IL} = GND	1, 2, 3	All	-10	+10	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	01-05		100	mA
				06		160	
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V V_O = 0.5 V	1, 2, 3	01-05	-30	-90	mA
				06	-30	-120	
Input capacitance	C_{IN} 4/ 5/	V_I = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT} 4/ 5/	V_O = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		10	pF
Functional testing		See 4.3.1e	7, 8	All			
Input or feedback to non-registered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
				06		10	
Clock to output	t_{CO}		9, 10, 11	01, 04		15	ns
				02		20	
				03		25	
				05		10	
				06		8	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF See figure 4, circuit A and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
				06		10	
Input to output disable	t_{ER}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
				06		10	
Clock period	t_P	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B, and figure 5	9, 10, 11	01	33		ns
				02	40		
				03	55		
				04	32		
				05	20		
				06	7		
Clock pulse width 4/ 6/	t_W		9, 10, 11	01, 04	15		ns
				02	20		
				03	27		
				05	6		
				06	3.5		
Setup time 4/ 6/	t_S		9, 10, 11	01	18		ns
				02	20		
				03	30		
				04	17		
				05	10		
				06	5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time 4/ 6/	t_H	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B,	9, 10, 11	All	0		ns
Maximum clock frequency 4/ 6/ $1/(t_{CO} + t_S)$	f_{MAX}	and figure 5	9, 10, 11	01	30		MHz
				02	25		
				03	18		
				04	31		
				05	50		
				06	77		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
				06	7		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
				06	8		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01, 04		25	ns
				02		30	
				03		40	
				05		20	
				06		14	
Power up reset time	t_{PR}		9, 10, 11	All		1.0	µs

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to registered outputs.

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Device types	01 through 06	
Case outlines	L and K	3 and X
Terminal number	Terminal symbol	
1	CP/I	NC
2	I	CP/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V_{CC}

FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CP/I	I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = Three-state
2. X = Don't care

FIGURE 2. Truth table.

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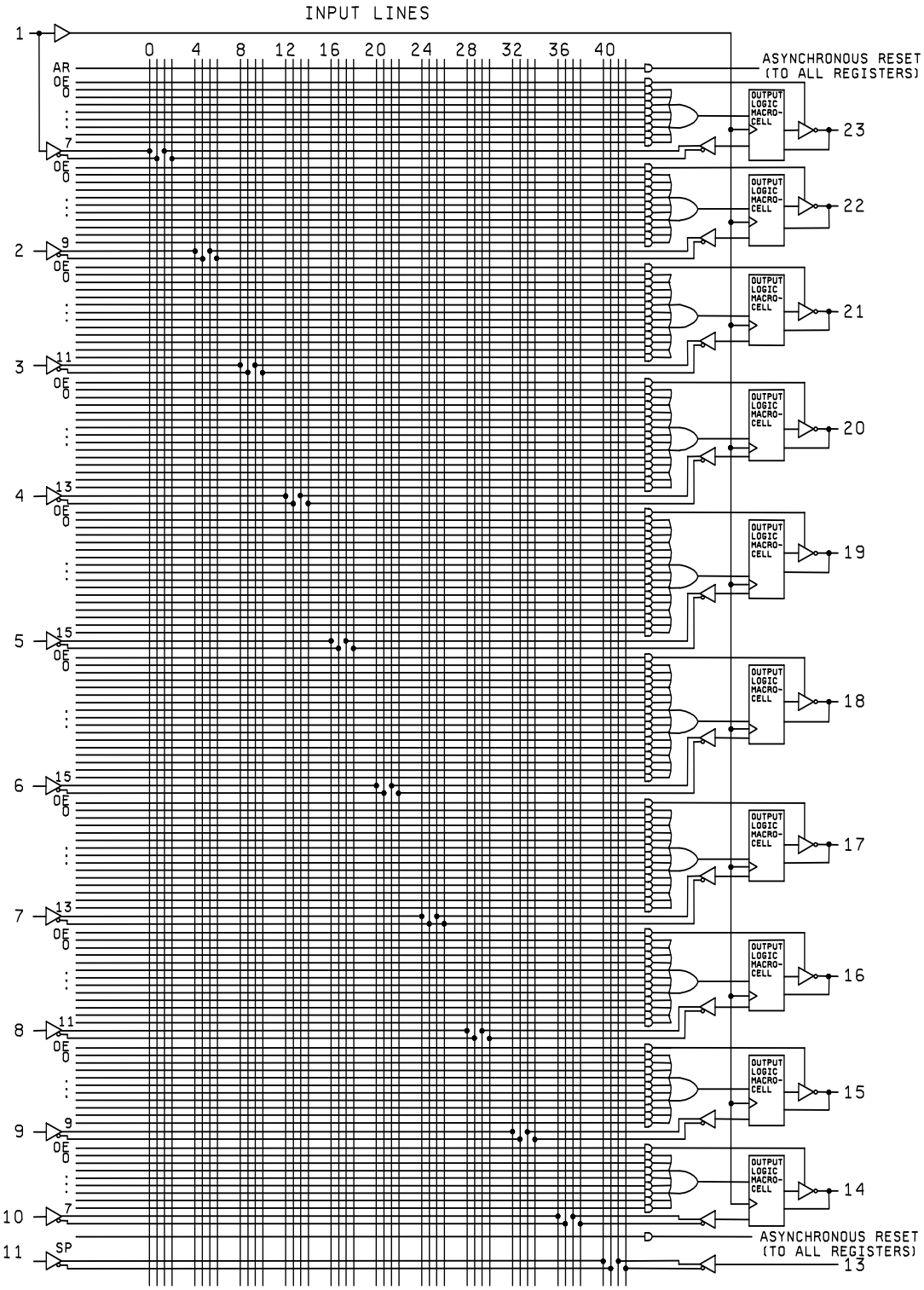

NOTE: PIN numbers apply to cases K and L only.

FIGURE 3. Logic diagram (unprogrammed).

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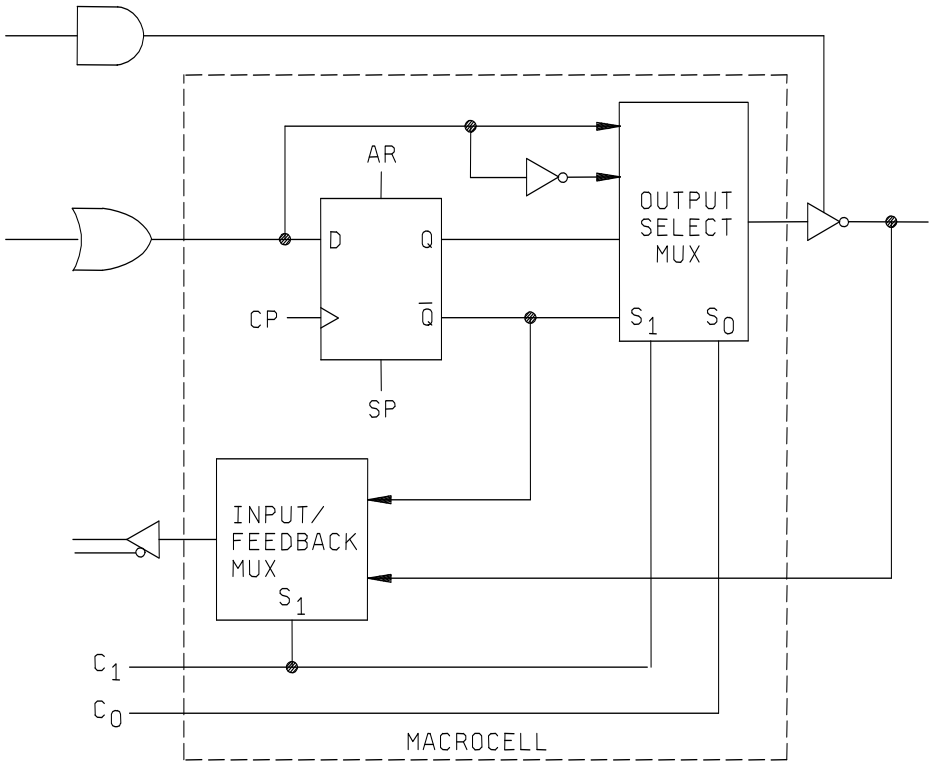

C_1	C_0	Output configuration
0	0	Registered/active low
0	1	Registered/active high
1	0	Combinatorial/active low
1	1	Combinatorial/active high

0 = Logical zero
1 = Logical one

FIGURE 3. Logic diagram (unprogrammed) - Continued.

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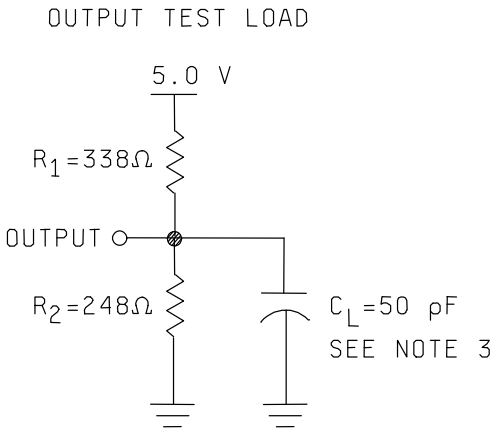
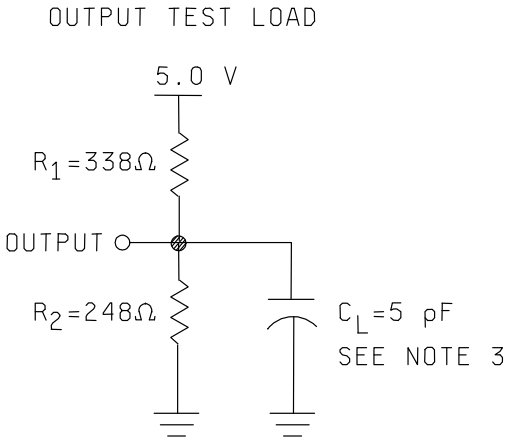


Circuit B or equivalent



Circuit A or equivalent (t_{EA} and t_{ER})

NOTES:
1. AC testing. Inputs pulse levels are 0 to 3.0 V with transition times of 5 ns or less. Timing reference levels are 1.5 V unless otherwise specified.
2. t_{EA} transition is measured ±500 mV from steady-state voltage.
3. Including jig and scope (minimum value).

FIGURE 4. Output test circuits.

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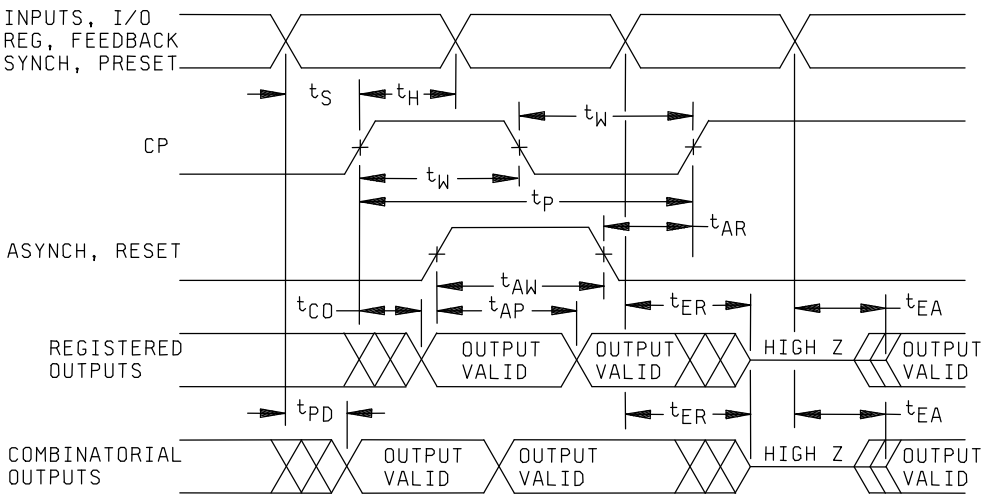

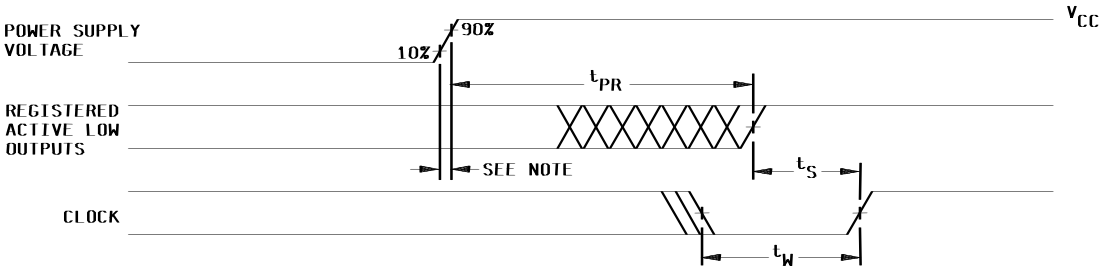

FIGURE 5. Switching waveforms.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. * Steps 1 through 3 may be performed at wafer level.

*(1) Program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

*(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or 2 hours at +300°C for unassembled devices only.

*(3) Perform margin test using V_m = +5.7 V minimum at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Perform margin test using V_m = +5.7 V at +25°C.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1). Devices may be submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.11.3).

* The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, or 2, 8A, 10

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7, 8A, and 8B, functional tests shall also verify no cells are programmed for unprogrammed devices or the altered item drawing pattern exists for programmed devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices submitted for testing shall be programmed in accordance with 3.2.3.1 or 3.2.3.2 herein or at the manufacturer's option; built-in test circuitry may be used to verify programmability and ac performance without programming the user array. After completion of all testing, the devices shall be erased and verified except devices submitted to groups C and D testing.

e. Subgroups 7, 8A, and 8B shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed in accordance with 3.2.3.1 or 3.2.3.2 herein. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 uW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedure. The programming procedure shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-03-29

Approved sources of supply for SMD 5962-87539 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8753901KA	3/	AT22V10-25YM/883
	0C7V7	PALC22V10-25TMB
5962-8753901LA	0C7V7	PALC22V10-25WMB
	3/	AT22V10-25DM/883
5962-87539013A	0C7V7	PALC22V10-25QMB
	3/	AT22V10-25LM/883
5962-8753902KA	3/	AT22V10-30YM/883
	0C7V7	PALC22V10-30TMB
5962-8753902LA	3/	AT22V10-30DM/883
	3/	PALC22V10H-30MQS/883B
	0C7V7	PALC22V10-30WMB
5962-87539023A	3/	AT22V10-30LM/883
	0C7V7	PALC22V10-30QMB
5962-8753903KA	3/	AT22V10-40YM/883
	0C7V7	PALC22V10-40TMB
5962-8753903LA	3/	AT22V10-40DM/883
	3/	PALC22V10H-40MQS/883B
	0C7V7	PALC22V10-40WMB
5962-87539033A	3/	AT22V10-40LM/883
	0C7V7	PALC22V10-40QMB
5962-8753904KA	3/	AT22V10-20YM/883
	0C7V7	PALC22V10B-20TMB
5962-8753904LA	0C7V7	PALC22V10B-20WMB
	3/	AT22V10-20DM/883
5962-87539043A	0C7V7	PALC22V10B-20QMB
	3/	AT22V10-20LM/883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8753905LA	3/	AT22V10-15DM/883
	0C7V7	PALC22V10B-15WMB
5962-87539053A	3/	AT22V10-15LM/883
	0C7V7	PALC22V10B-15QMB
5962-8753905KA	3/	AT22V10-15YM/883
	0C7V7	PALC22V10B-15TMB
5962-8753906LA	3/	AT22V10B-10DM/883
5962-87539063A	3/	AT22V10B-10LM/883
5962-8753906XA	3/	AT22V10B-10KM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address	Margin test method
0C7V7	QP Semiconductor 2945 Oakmead Village Ct. Santa Clara, CA 95051	A

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